08/27/2002 10/022,297

27aug02 15:17:19 User267149 Session D297.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2002/Aug W4
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*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2002/Sep W2
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File 34:SciSearch(R) Cited Ref Sci 1990-2002/Aug W4
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*File 34: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2002/Aug
(c) 2002 ProQuest Info&Learning
File 65:Inside Conferences 1993-2002/Aug W4
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File 77:Conference Papers Index 1973-2002/Jul
(c) 2002 Cambridge Sci Abs
File 94:JICST-EPlus 1985-2002/Jun W5
(c)2002 Japan Science and Tech Corp(JST)
*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Jul
(c) 2002 The HW Wilson Co.
File 108:AEROSPACE DATABASE 1962-2002/Aug
(c) 2002 AIAA
File 144:Pascal 1973-2002/Aug W4
(c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Aug
(c) 2002 Cambridge Scient. Abstr
File 305:Analytical Abstracts 1980-2002/Aug W2
(c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2002/Jul
(c) 2002 DECHEMA
File 350:Derwent WPIX 1963-2002/UD,UM &UP=200254
(c) 2002 Thomson Derwent
*File 350: Alerts can now have images sent via all delivery methods. See HELP ALERT and HELP PRINT for more info.
File 344:Chinese Patents Abs Aug 1985-2002/Aug
(c) 2002 European Patent Office
File 347:JAPIO Oct 1976-2002/Apr(Updated 020805)
(c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.

08/27/2002 10/022,297

Alerts have been run. See HELP NEWS 347 for details.
File 371:French Patents 1961-2002/BOPI 200209
(c) 2002 INPI. All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.

STIC-EIC 2800 CP4-9C18 Irina Speckhard 308-6559

Set	Items	Description
S1	596220	(SEMICONDUCT?????(N1)DEVICE? ?)
S2	2434405	SEMICONDUCT?????
S3	7265	CC=B2560 Semiconductor devices
S4	4997	MC=S01-G02B
S5	99381	IC=G01R-031
S6	2512168	S1:S5
S7	1929185	SUBSTRATE? ?
S8	224791	CC=(A6855 OR A8115 OR B0520 OR B2220 OR B2570)
S9	2944	MC=(T03-A01B OR T03-A01B1 OR T03-A01B)
S10	5762	IC=G11B-005/704
S11	2083719	S7:S10
S12	3089757	ALUMINIUM OR ALUMINUM OR AL OR MOLTEN OR PYROPHORIC
S13	7359567	LAND OR LAYER???? OR COAT????? OR FILM?????
S14	1424809	COPPER OR CU
S15	3178564	CHIP? ? OR LEAD? ? OR FRAME? ?
S16	559017	RECTANG?????? OR (RIGHT(3N)ANGLE??)
S17	67734	S15 AND S16
S18	187332	(SYNTHET?????? OR ARTIFIV??????)(3N)(EPOX??? OR RESIN? ? OR THERMOPLASTIC??? OR ELASTOMER?? OR RUBBER? ? OR ADHESIVE??)
S19	2859211	EPOX??? OR RESIN? ? OR THERMOPLASTIC??? OR ELASTOMER?? OR RUBBER? ? OR ADHESIVE??
S20	99574	POLYIMIDE? ? OR POLYIMIDO
S21	21399	IMIDO OR IMIDE???(2N)POLYMER???
S22	666	MC=V04-R07C
S23	240359	RESIN???(N3)(LAYER????? OR FILM??? OR COAT???)
S24	2925016	POLYMER? ? OR HOMOPOLYMER? ? OR COPOLYMER? ?
S25	4792439	S18:S24
S26	86344	COEFFICIENT? ?(3N)(EXPANS?????? OR EXPAND??????)
S27	536388	S6 AND S11
S28	64503	S27 AND S12
S29	53739	S28 AND S13
S30	3830	S29 AND S14
S31	4	S30 AND S17
S32	4	RD (unique items)
S33	3826	S30 NOT S31
S34	749	S33 AND S25
S35	34	S34 AND S26
S36	29	S35 AND S19
S37	29	RD (unique items)
S38	28	IDPAT (sorted in duplicate/non-duplicate order)
S39	28	IDPAT (primary/non-duplicate records only)
S40	204170	S11 AND S12
S41	353275	S13 AND S14
S42	18544	S41 AND S40
S43	324	S42 AND S26
S44	296	S43 NOT S39
S45	1	S44 AND S18
S46	295	S44 NOT S45
S47	83	S46 AND S6
S48	2	S47 AND S19
S49	81	S47 NOT S48
S50	0	S49 AND CORNER???

S51	8	S49 AND (SOLDER??????(3N)(LAYER??? OR FILM??? OR COAT???))
S52	8	RD (unique items)
S53	73	S49 NOT S51
S54	12	S53 AND SOLDER???????
S55	12	RD (unique items)

32/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014342404
WPI Acc No: 2002-163107/200221
XRAM Acc No: C02-050281
XRPX Acc No: N02-124466
Low-profile **semiconductor device**, e.g. ball grid array device, includes second encapsulant formed to encapsulate solder balls or lumps with bottom ends exposed to and flush with bottom surface of second encapsulant
Patent Assignee: UNITED TEST CENT INC (UNTE-N)
Inventor: BAI J; TSAI C
Number of Countries: 027 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6326700	B1	20011204	US 2000639202	A	20000815	200221	B
EP 1205973	A1	20020515	EP 2000124579	A	20001110	200239	N

Priority Applications (No Type Date): US 2000639202 A 20000815; EP 2000124579 A 20001110
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6326700	B1		11	H01L-023/29	
EP 1205973	A1	E		H01L-023/31	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): US 6326700 B1
Abstract (Basic):

NOVELTY - A low-profile **semiconductor device** has a **substrate**, a **semiconductor** die, gold wires and solder balls or lumps, and two encapsulants. The second encapsulant is formed over the conductive traces of the **substrate** to encapsulate the conductive traces, gold wires, a hole, and solder balls or lumps with bottom ends exposed to or flush with a bottom surface of the second encapsulant.

DETAILED DESCRIPTION - A low-profile **semiconductor device** comprises a **substrate** (41), a **semiconductor** die (40), gold wires and solder balls or lumps, and two encapsulants. The **substrate** has a base **layer** and conductive traces formed on the base **layer**. The base **layer** is formed with at least a hole. The **semiconductor** die has an active surface and an opposing inactive surface. It is mounted on the base **layer** of the **substrate** via the active surface. The gold wires pass through the hole in the **substrate** for electrically coupling the **semiconductor** die to the conductive traces on the **substrate** . The solder balls or lumps are arranged on terminals of the conductive traces for electrically connecting the **semiconductor** die to external devices. The first encapsulant is formed on the **substrate** to encapsulate the **semiconductor** die. The second encapsulant is formed over the conductive traces of the **substrate** to encapsulate the conductive traces, the gold wires, and the hole. It

is also formed to encapsulate solder balls or lumps with bottom ends exposed to and flush with the bottom surface of the second encapsulant. An INDEPENDENT CLAIM is also included for a method of manufacturing a low-profile **semiconductor device**.

USE - As low-profile **semiconductor device**, e.g. ball grid array devices.

ADVANTAGE - The device has a reduced overall thickness. It eliminates warpage of the device such that the occurrence of delamination between the **semiconductor** die and the **substrate** can be effectively prevented. It can improve the accuracy of testing of electrical performance. It can be electrically connected to an external device in a quality-assured way than the prior art. The **substrate** of the device needs not to be **coated** with solder mask, thus reducing the cost for making the **substrate** .

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view of a **semiconductor device**.

semiconductor die (40)
substrate (41)
upper encapsulant (43)
heat spreader (46)
top surface (430)
pp; 11 DwgNo 6/11

32/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010760325
WPI Acc No: 1996-257280/199626
XRPX Acc No: N96-216429
Heat-dissipation fin for **semiconductor** package, hybrid integrated circuit **substrate** - has several metal fins made by bending **rectangular** metal plates whose bases are connected to several pores formed on metal board using solder or adhesive
Patent Assignee: MITSUBISHI MATERIALS CORP (MITV)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8107166	A	19960423	JP 94241722	A	19941006	199626	B

Priority Applications (No Type Date): JP 94241722 A 19941006
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8107166	A		7	H01L-023/36	

Abstract (Basic): JP 8107166 A

The fin (11) includes a metal structures (22) formed by bending thin **rectangular** metal plates. The bases (22a) of the metal structures are attached to several pores (21a) formed on a metal board (21) using a solder (14) or an adhesive agent.

The metal board consisting of an alloy of **Cu**, W , and Ni connects to the back surface of a ceramic **layer** (16). The ceramic **layer** serves as the bottom **substrate** of a **semiconductor device** (13) and consists of an **Al** metal. The metal board has an area which can cover a thermal expansion coefficient equivalent to the ceramic **layer**. A **semiconductor chip** (12) mounts the other surface of the ceramic **layer**.

USE/ADVANTAGE - Also for e.g power module **substrate**. Dissipates heat generated by **semiconductor chip**. Prevents ceramic **substrate** and metal board from breaking and metal fin from deforming.

Dwg.1/6

32/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010160715
WPI Acc No: 1995-061968/199509
XRPX Acc No: N95-049374
Semiconductor wafer with multiple device areas and alignment mark - uses recesses and projections as alignment mark, e.g. in insulator **film**, and has recess or projection width smaller than average particle size of metal **film** grains on alignment mark
Patent Assignee: TOSHIBA KK (TOKE)
Inventor: ABE M; HARAGUCHI H; NOMURA W
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 631316	A2	19941228	EP 94109632	A	19940622	199509	B
JP 7135172	A	19950523	JP 94132020	A	19940614	199529	
US 5532520	A	19960702	US 94263333	A	19940621	199632	
EP 631316	A3	19970226	EP 94109632	A	19940622	199717	
US 5786267	A	19980728	US 94263333	A	19940621	199837	
			US 95456695	A	19950601		
KR 139702	B1	19980715	KR 9414237	A	19940622	200018	
JP 3034428	B2	20000417	JP 94132020	A	19940614	200024	

Priority Applications (No Type Date): JP 93150431 A 19930622
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 631316	A2	E	33	H01L-023/544	
Designated States (Regional): DE FR GB					
JP 3034428	B2		20	H01L-021/027	Previous Publ. patent JP 7135172
JP 7135172	A		21	H01L-021/027	
US 5532520	A		29	H01L-023/544	
US 5786267	A			H01L-021/44	Div ex application US 94263333 Div ex patent US 5532520
KR 139702	B1			H01L-021/027	
EP 631316	A3			H01L-023/544	

Abstract (Basic): EP 631316 A

The wafer alignment mark includes at least one recess or projection, and is formed in a wafer area other than the device areas. There is a metal **film** on the alignment mark, and the recess or projection is narrower than the average grain size of the metal **film**. The recesses and projections are repetitively formed in the row direction.

Pref. the alignment mark is formed in either or both a dicing line or an orientation flat area. There are pref. multiple parallel marks, with a **rectangular**, L or cross shape. The alignment mark recesses may be slit holes on an insulating **layer** on the wafer **substrate**, and the projections may be wall-like insulating **layers** on the **substrate**.

USE/ADVANTAGE - In reduction projection exposure aligner; for X-direction; allows mark detection by stepper even with planarised metal **film** on mark.

Dwg.12/45

Abstract (Equivalent): US 5532520 A

<E8-Abstract PN=5532520>

Disclosed is an alignment mark for the X directional alignment of a **chip** area on a **semiconductor** wafer, for example. The alignment mark comprises recesses and projections formed on a **semiconductor substrate**. The recesses or projections are repeatedly arranged in the X direction. The X directional width of the recesses or projections is set smaller than the X directional width of a grain on a metal **film** formed on the recesses and projections or the average particle size, as viewed from above the **semiconductor substrate**. The projections may be formed by a insulating **layer** formed on the **semiconductor substrate**.

<E3-Claims PN=5532520>

What is claimed is:

1. A **semiconductor device** comprising:

a **semiconductor** wafer having a plurality of device areas;

at least one alignment mark comprising a recess formed on said **semiconductor** wafer; and

a metal **film** formed on said alignment mark, said recess of said alignment mark having a width smaller than an average size of gains of said metal **film**.

2. The **semiconductor device** according to claim 1, wherein said alignment mark is formed on a dicing line extending among the device areas.

3. The **semiconductor device** according to claim 1, wherein said at least one alignment mark is formed in one of areas other than the device areas.

4. The **semiconductor device** according to claim 1, wherein a planar shape of said alignment mark is one of a **rectangular** shape, an I shape, an L shape and a cross shape5. The **semiconductor device** according to claim 1, wherein said alignment mark is made of one of an insulating **film** including a silicon oxide **film** or a silicon nitride **film**, and a conductive **film** including a polysilicon **film**.

6. The **semiconductor device** according to claim 1, wherein there are a plurality of alignment marks arranged in parallel to one another.

7. The **semiconductor device** according to claim 5, wherein an interval between adjoining alignment marks is smaller than said average size of said grains of said metal **film**.

8. The **semiconductor device** according to claim 1, wherein there are a plurality of alignment marks arranged in a matrix form.

9. The **semiconductor device** according to claim 1, wherein said average size of said grains of said metal **film** is determined by

2multiplied by(S/npi)one half

where S is a unit area at an arbitrary position on said **semiconductor substrate** and n is a number of grains of a metal **film** included in said unit area S.

10. The **semiconductor device** according to claim 1, wherein said average size of said grains of said metal **film** is determined by

32/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002283488
WPI Acc No: 1979-82696B/197946
Electromagnetic induction device for sintering **coating** on **substrate** - has **rectangular** induction coil with rounded corners, giving uniform alloying
Patent Assignee: SIEMENS AG (SIEI)
Inventor: KELLER H; RAAB H; STRACK H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 2818940	A	19791108				197946	B
JP 54143066	A	19791107				197950	

Priority Applications (No Type Date): DE 2818940 A 19780428; DE 543443 A 19780518

Abstract (Basic): DE 2818940 A

Device uses a **rectangular** induction coil with rounded corners, the max. dimension of the winding cross-section being greater than the min. dimension of the **substrate** used. As uniform alloying as possible with low alloyed depth is obtd. at all points of the **substrate** to be sintered, whilst sintering times are slight. The process can be automated.

The **substrate** has a mobile support (conveyer belt), which makes it possible to move the **substrate** parallel to the winding cross-section of the coil and at a fixed distance from the coil. The support moves at a speed of 1-50 mm/s. It is provided with **frames** damping electromagnetic radiation at a fixed distance from the coil, these **frames** consisting of metal (alloy), esp. **Cu**, Ag, Au, Ti, **Al**, Cr, Ni or their alloys or alloys of **semiconductors**. Sintering is carried out under a protective gas, e.g. N2 and/or H2, esp. a mixt of 90% N2 and 10% H2.

39/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014599583
WPI Acc No: 2002-420287/200245
XRAM Acc No: C02-119141
XRPX Acc No: N02-330606
Ceramic module for mounting power device, has ceramic **substrate** containing specific composite material joined with wiring and/or cooling plate through joining material, and metallize **layer** formed on **substrate**
Patent Assignee: SUMITOMO METAL IND LTD (SUMQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002043481	A	20020208	JP 2000219573	A	20000719	200245	B

Priority Applications (No Type Date): JP 2000219573 A 20000719
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002043481	A		8	H01L-023/373	

Abstract (Basic): JP 2002043481 A
Abstract (Basic):
NOVELTY - The ceramic module has ceramic **substrate** (4) in which surface(s) is joined with wiring (1) and/or cooling plate (5) through a joining material (2). **Substrate** contains composite material chosen from 2 types or more of magnesium oxide (MgO), MgO spinel and MgO, MgO spinel, and **aluminum** oxide. A metallize **layer** (3) having a material with preset thermal **expansion coefficient** is formed in surface(s) of **substrate**.

DETAILED DESCRIPTION - The wiring and cooling plate, each consists of **copper** as main component. The metallize **layer** has a material with thermal **expansion coefficient** smaller than that of cooling plate. The wiring and cooling plate, are joined through a joining material (2) having heat conductivity of 1W/m.K or more. The joining material is chosen from a solder, brazing material and **resin**. An INDEPENDENT CLAIM is also included for ceramic module manufacture.

USE - For mounting large **semiconductor** element of heating value like power **semiconductor device**.

ADVANTAGE - The ceramic module having excellent heat release (cooling) property, is obtained using the ceramic **substrate**. The ceramic module suitable for mounting large **semiconductor** element of heating value like power device is provided economically. The reliability of the junction portion is high.

DESCRIPTION OF DRAWING(S) - The figure shows the explanatory drawing of cross-section of the ceramic module.

Wiring (1)
Joining **layer** (2)
Metallize **layer** (3)
Ceramic **substrate** (4)
Cooling plate (5)

39/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014560925
WPI Acc No: 2002-381628/200241
Related WPI Acc No: 2002-235478; 2002-478453
XRAM Acc No: C02-107582
XRPX Acc No: N02-298637
Fabrication of **semiconductor device** assembly comprises attaching stabilizing plate to **substrate** adjacent ball grid array structure
Patent Assignee: MICRON TECHNOLOGY INC (MICR-N)
Inventor: GOOCH S; WENSEL R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020019080	A1	20020214	US 99251252	A	19990216	200241 B
			US 2001954552	A	20010917	

Priority Applications (No Type Date): US 99251252 A 19990216; US 2001954552 A 20010917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020019080	A1		10	H01L-021/44	Div ex application US 99251252 Div ex patent US 6291899

Abstract (Basic): US 20020019080 A1
Abstract (Basic):
NOVELTY - A **semiconductor device** assembly is fabricated by:
(i) securing a **semiconductor** chip to a **substrate** surface;
(ii) coupling a ball grid array (BGA) structure to an opposing **substrate** surface;
(iii) attaching a stabilizing plate to the **substrate** adjacent the BGA structure; and
(iv) encapsulating the chip and a **substrate** portion adjacent the chip.
USE - For fabricating a **semiconductor device** (preferably BGA) assembly.
ADVANTAGE - The use of stabilizing plate increases the reliability and manufacturability of the BGA assembly, and provides a cost-efficient and effective reduction of assembly warpage.
DESCRIPTION OF DRAWING(S) - The figure shows steps in fabricating a BGA assembly.
pp; 10 DwgNo 5/5

39/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014470534
WPI Acc No: 2002-291237/200233
Related WPI Acc No: 2002-146918
XRAM Acc No: C02-085380
XRPX Acc No: N02-227388
IC device testing apparatus has probe tip placed on contact locations of test **substrate**, which is supported by **polymer** sheet having holes aligned with probe tip
Patent Assignee: BEAMAN B S (BEAM-I); FOGEL K E (FOGE-I); LAURO P A (LAUR-I); NORCOTT M H (NORC-I); SHIH D (SHIH-I); WALKER G F (WALK-I)
Inventor: BEAMAN B S; FOGEL K E; LAURO P A; NORCOTT M H; SHIH D; WALKER G F
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20020011001	A1	20020131	US 98198179	A	19981123	200233 B
			US 2001972622	A	20011010	

Priority Applications (No Type Date): US 98198179 A 19981123; US 2001972622 A 20011010
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020011001	A1		12	H05K-001/03	Div ex application US 98198179

Abstract (Basic): US 20020011001 A1
Abstract (Basic):
NOVELTY - Probe tips (13) are arranged on contact locations on a test **substrate** (10) which includes electro conductor patterns, a decoupling capacitor and elongated electrical conductors. Holes in a **polymer** sheet (40) supporting the probe tip, are aligned with the probe tips. When the **substrate** is moved towards integrated circuit (IC) device, solder balls on the IC device are receiving in the holes.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) (i) High density integrated rigid test probe fabrication method which involves bonding elongated electrical conductor to a **substrate** by forming a ball bond on the **substrate**. The elongated electrical conductor is sheared from ball bond and the exposed conductor end is flattened. The elongated conductor extends within holes in a **polymer** sheet on which another **polymer** sheet with holes is formed. The **substrate** is moved towards workpiece so that the elongated electrical conductors are placed in contact with conductors on the IC device; (ii) High density integral rigid test probe which includes short studs extending from ball bonds attached to contact locations of a fan out **substrate** which is selected from the group consisting of multi **layer** ceramic **substrate** with thick **film** wiring, multi **layer** ceramic **substrate** with thin **film** wiring, metallized ceramic **substrates** with thin **film** wiring, **epoxy** glass

laminate **substrates** with **copper** wiring and silicon **substrates** with thin **film** wiring. The ball bonds and short studs are surrounded by a **polymer** sheet having **coefficient** of thermal **expansion** that is matched to the fan out **substrate** and has a glass transition temperature greater than 200 degrees C. Another **polymer** sheet with enlarged holes is formed over the **polymer** sheet. Two metal **layers** are formed on enlarged contact surface at the end of the studs to inhibit oxidation and diffusion of the temperatures up to 200 degrees C and to prevent out-diffusion of the underlying material

USE - For electrically testing an IC device and other electronic components that use solder balls for interconnection.

ADVANTAGE - The enlarged holes in the **polymer** sheet acts as a cup to control and contain the creep of the solder balls at high temperatures. The cup-shaped geometry of the probe facilitates alignment of solder balls with probe contact.

DESCRIPTION OF DRAWING(S) - The drawing shows the probe fabrication process.

test **substrate** (10)

probe tip (13)

polymer sheet (40)

pp; 12 DwgNo 7/12

39/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014433572
WPI Acc No: 2002-254275/200230
XRAM Acc No: C02-075946
XRPX Acc No: N02-196367
High thermal conductivity **layer** for use in optoelectronic device e.g., laser diode comprises adhesion **layer**, dielectric waveguide **layer**, highly heat conductive **layer**, and stress compensation **layer**
Patent Assignee: UNIV CALIFORNIA (REGC)
Inventor: DERI R J; DIJAILI S P; GOWARD W; PATTERSON F G; PETERSEN H; WALKER J D
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6347106	B1	20020212	US 99257288	A	19990225	200230	B

Priority Applications (No Type Date): US 99257288 A 19990225
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6347106	B1		8	H01S-005/223	

Abstract (Basic): US 6347106 B1
Abstract (Basic):
NOVELTY - A high thermal conductivity **layer** includes an adhesion **layer**, and a dielectric waveguide **layer** connected to the adhesion **layer**. A highly heat conductive **layer** is connected to the dielectric waveguide **layer**. A stress compensation **layer** is provided on the highly heat conductive **layer** to compensate for the **film** stress built up in the adhesion **layer** and the heat conductive **layer**.
DETAILED DESCRIPTION - A high thermal conductivity (HTC) **layer** (24) for use in an optoelectronic device includes an adhesion **layer** for binding III-V oxides with materials of the optoelectronic device that are adjacent to the adhesion **layer**. A dielectric waveguide **layer**, which provides optical confinement for a guided optical mode, is fixedly connected to the adhesion **layer**. A highly heat conductive **layer** is fixedly connected to the dielectric **layer** waveguide **layer**. The conductive **layer** is highly heat conductive relative to the material within the optical gain region of the optoelectronic device in which the HTC **layer** is located. A stress compensation **layer** is provided on the highly heat conductive **layer** to compensate for the **film** stress built up in the adhesion **layer** and the highly heat conductive **layer**. The stress compensation **layer** reduces the tendency of the adhesion **layer** and the highly heat conductive **layer** to delaminate due to differences in thermal **expansion coefficients**.
An INDEPENDENT CLAIM is also included for a laser comprising an optically active region. A highly thermally conductive Bragg mirror is provided to reflect laser light generated within the optically active

region back towards the optically active region. A first region, which provides current carrier injection into the optically active region, is fixedly attached between the optically active region and the Bragg mirror. A second region, which provides current injection of the opposite carrier type to that of the first region, is fixedly attached to the optically active region on a side opposite to the side of the optically active region where the first region is attached. By injecting carriers of opposite polarities into the optically active region, a population inversion is created and optical gain is provided. A second Bragg mirror is provided which is also adapted to reflect laser light generated within the optically active region back towards the optically active region. A **semiconductor substrate** is fixedly connected to the second Bragg mirror. A first ohmic contact is connected to the wall of the highly thermally Bragg mirror and to the first region. A second ohmic contact is connected to the **semiconductor substrate**. A source of electrical current may be connected to the first ohmic contact and the second ohmic contact to provide electrical current to the laser. A heat sink is connected to the highly thermally conductive Bragg mirror and to the first ohmic contact.

USE - The invention is used in optoelectronic devices e.g., laser diodes, light emitting diodes, and ridge waveguide **semiconductor** optical amplifier. It can be used in a Bragg mirror in the construction of a vertical cavity **semiconductor** laser diode.

ADVANTAGE - The inventive HTC **layer** exhibits low optical loss, and is capable of enhancing the conduction of heat away from the active region of the optoelectronic device, thus improving the device performance.

DESCRIPTION OF DRAWING(S) - The figure shows a ridge waveguide incorporating the high thermal conductivity **layer**.

HTC **layer** (24)

pp; 8 DwgNo 2/3

39/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014394859
WPI Acc No: 2002-215562/200227
XRAM Acc No: C02-065809
XRPX Acc No: N02-165117
Mounting of one or more wire bond integrated circuit chips by creating interface **substrate** overlying metal **substrate** comprises creating build up multilayer **layer** over interconnect **layer**
Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010046725	A1	20011129	US 99389634	A	19990903	200227 B
			US 2001900558	A	20010709	

Priority Applications (No Type Date): US 99389634 A 19990903; US 2001900558 A 20010709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010046725	A1		12	H01L-021/44	Div ex application US 99389634

Abstract (Basic): US 20010046725 A1
Abstract (Basic):

NOVELTY - Mounting of one or more wire bond integrated circuit chips by creating an interface **substrate** overlying a metal **substrate** comprises: providing wire bond chip(s) and metal **substrate**; creating build up multilayer; masking and etching the **substrate**; selectively creating openings; inserting chips into openings; wire bonding the chips; and inserting solder balls to ball grid array solder connections.

DETAILED DESCRIPTION - Mounting of one or more wire bond integrated circuit chips (16) by creating an interface **substrate** overlying a metal **substrate** (14) comprises:

(a) providing one or more wire bond chips having pads for wire bond connections;

(b) providing a metal **substrate** having first and second surfaces (24, 26);

(c) cleaning the first surface of the metal **substrate**;

(d) depositing a **layer** of dielectric over the first surface;

(e) depositing an interconnect **layer** over the dielectric **layer** to form the first **layer** of an interconnect **substrate** (12);

(f) creating a build up multilayer (BUM) **layer** over the interconnect **layer** to form the second **layer** of interconnect **substrate**;

(g) masking and etching the second surface of the metal **substrate** to create one or more openings (28) for the insertion of one or more bond chips to furthermore expose portions of the dielectric within the openings;

(h) selectively creating openings in the exposed dielectric to

provide electrical access and heat removal to the interconnect **substrate** for the wire bond chip(s);

(i) subdividing the metal **substrate** into individual wire bond **substrates**;

(j) **coating** the exposed dielectric of the individual wire bond **substrates** with a **layer** of **adhesive** (17);

(k) inserting wire bond chip(s) into opening(s) for the insertion of the wire bond chips in the individual wire bond **substrates** where the wire bond chips overlay the **adhesive coating**;

(l) wire bonding the wire bond chips to the selectively created openings in the dielectric;

(m) inserting a molding compound over the wire bond chip(s) within the opening(s) for the insertion of the wire bond chips;

(n) **coating** the BUM **layer** as a solder mask;

(o) exposing the metal pads within the BUM **layer** to create openings for the ball grid array (BGA) solder connections; and

(p) inserting and attaching solder balls (10, 11) to the BGA solder connections.

An INDEPENDENT CLAIM is also included for a structure for mounting one or more wire bond IC chips by creating an interface **substrate** overlying a metal **substrate** comprising:

(i) metal **substrate** having first and second surfaces;

(ii) **layer** of dielectric with a thickness of 10-50 microns deposited over the first surface;

(iii) thin **film** interconnect **layer** deposited over the **layer** of dielectric to form a first **layer** of an interconnect **substrate**;

(iv) BUM **layer** created over the interconnect **layer** to form the second **layer** of an interconnect **substrate**; (v) opening(s) for the insertion of wire bond chip(s) created by masking and etching the second surface of the metal **substrate** to furthermore create exposed portions of the dielectric within the openings;

(vi) openings selectively created in the exposed dielectric to provide electrical access and heat transfer to the interconnect **substrate** for the wire bond chip(s);

(vii) individual wire bond **substrates** created by subdividing the metal **substrate**;

(viii) **layer** of **adhesive** containing thermally conductive **epoxy** such as thermoset or **thermoplastic epoxy** created by **coating** the exposed dielectric of the individual wire bond **substrates**;

(ix) wire bond chip(s) inserted into the opening(s) for the insertion of the wire bond chips in the individual wire bond **substrates** where the wire bond chips overlay the **adhesive coating**;

(x) wire bonds for the wire bond chips to the selectively created openings in the dielectric;

(xi) molding compound inserted over the wire bond chip(s) and within the opening(s) for the insertion of the wire bond chips;

(xii) **coating** over the BUM **layer** as a solder mask;

(xiii) metal pads within the BUM **layer** created by etching to create openings for the BGA solder connections; and

(xiv) solder balls inserted and attached to the BGA solder

connections.

USE - The method is used for mounting one or more wire bond integrated circuit chips to create packaging **substrates** that are used for wire bonded **semiconductor devices**.

ADVANTAGE - The method is inexpensive and reliable for high-density wire bond **semiconductor device** manufacturing. The wire bond package significantly improves the cooling of the IC device that is mounted. The method provides for high pin fan-out for wire bond **semiconductor devices**. The need for counter-balancing the effects of thick **layers** of dielectric used in conventional high-density wire bond **semiconductor device** manufacturing is eliminated. The method provides an initial surface with good planarity for the creation of high-density wire bond **semiconductor** structures. The structure used for mounting the wire bond IC chip(s) is devoid of warpage and dimensional variations during high temperature or wet chemical processing for the creation of high-density wire bond **semiconductor** structures.

DESCRIPTION OF DRAWING(S) - The figure shows a single chip wire bond chip package with two interconnect **layers**.

Solder balls (10, 11)
Interconnect **substrate** (12)
Metal **substrate** (14)
Wire bond chip (16)
Adhesive layer (17)
First and second surfaces (24, 26)
Opening(s) (28)
pp; 12 DwgNo 1/3

39/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014056782
WPI Acc No: 2001-540995/200160
Related WPI Acc No: 2002-040077
XRAM Acc No: C01-161404
XRPX Acc No: N01-402090
Mounting of flip chip on metal **substrate**, involves forming opening on exposed build-up multi-**layer** on one side, and openings on other side of **substrate**, **adhesive coating** exposed **epoxy** of divided chip, connecting chips
Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010016370	A1	20010823	US 99419512	A	19991018	200160 B
			US 2001846539	A	20010502	

Priority Applications (No Type Date): US 99419512 A 19991018; US 2001846539 A 20010502
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010016370	A1		13	H01L-021/44	Div ex application US 99419512

Abstract (Basic): US 20010016370 A1
Abstract (Basic):
NOVELTY - **Epoxy layer** is formed on surface A of **substrate** (14). Build-up multi-**layer** (BUM) on **epoxy layer** is exposed to form openings. Openings for integrated circuit (IC) chip are formed on surface B of **substrate**. Openings are created selectively in exposed **epoxy**. **Substrate** is subdivided, the exposed **epoxy** of chip is **coated** with **adhesive**, and chips are connected. Molding compound is applied on chips, and solder balls are inserted.
DETAILED DESCRIPTION - One or more integrated circuit (IC) chips having pads for electric connections are provided. A metal **substrate** (14) having first and second surfaces (24,26) is provided. The first surface of the metal **substrate** is cleaned and **epoxy layer** is deposited on the first surface of the **substrate**. An interconnect **layer** (20) is deposited on **epoxy layer** to form first **layer** of interconnect **substrate** (12). A build up multi-**layer** (BUM) is formed on the interconnect **layer** to form second **layer** of interconnect **substrate**. The BUM **layer** is **coated** with solder mask. The metal pads within BUM **layer** are exposed to create openings (32,33) for ball grid array (BGA) solder connections. The second surface of metal **substrate** is masked and etched to form one or more openings (28) for insertion of the IC chips. The portions of **epoxy** are exposed further within the openings. Openings are selectively created in exposed **epoxy** to provide electrical access

and heat removal to interconnect **substrate**. The metal **substrate** is subdivided into individual IC chip **substrates**. The exposed **epoxy** of individual IC chip **substrate** is **coated** with **adhesive layer** (17) for wire bond die. The **adhesive** is not required for flip chip die. One or more IC chips are inserted into one or more openings in individual IC chips **substrates**. A wire bonded IC chip is provided on **adhesive coating**. The IC chips are electrically connected through selectively created openings in **epoxy** by wire bond or reflow solder for flip chip case. A molding compound (22) is applied on IC chips. Solder balls (10,11) are inserted and attached to BGA solder connections.

INDEPENDENT CLAIMS are also included for the following:

(i) a structure for mounting one or more integrated circuit chips within a metal **substrate**; and

(ii) an interconnect structure comprising one or more insulating **films** and one or more conductive patterns.

The insulating **films** comprise **epoxy** material which is deposited or laminated on the **substrate** which is subsequently removed in part. The insulation **film** is used in suspension or in decal mode.

USE - For mounting IC chips such as wire bond and flip chip within metal **substrate** (claimed) for producing printed circuit boards which are used in the manufacture of large **semiconductor** functional units.

ADVANTAGE - Inexpensive and reliable method of high-density wire bond and flip chip **semiconductor device** manufacture is provided. The wire bond and flip chip device package significantly improves the cooling of mounted IC device. High pin fan-out for wire bond and flip chip **semiconductor devices**, is provided. The need for counter-balancing the effects of thick **layers** of dielectric for **semiconductor device** manufacture, is eliminated. The high density wire bond and flip chip **semiconductor devices** are packaged using BUM technology in combination with thin **film** deposition techniques. The high-density wire bond and flip chip **semiconductor** structures have good planarity initial surfaces. High-density wire bond and flip chip **semiconductor** structures are easily formed from structure devoid of warpage and dimensional variations by high temperature or wet chemical processing. A new method for mounting high-density wire bond **semiconductor device** is provided. The low cost, wide availability and versatility **epoxy** has thermal **coefficient** of **expansion** (TCE) higher than that of the metal **substrate**. The **film** which is present in the bottom of the cavity is stretched taut, and the **film** absorbs little water to provide a stable surface that does not sag or deform.

DESCRIPTION OF DRAWING(S) - The figure shows a single chip wire bond chip package to interconnect **layers**.

Solder balls (10,11)
Interconnect **substrate** (12)
Metal **substrate** (14)
Adhesive layer (17)
Interconnect **layer** (20)
Molding compound (22)

39/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013972136
WPI Acc No: 2001-456349/200149
XRAM Acc No: C01-137934
XRPX Acc No: N01-338137
Semiconductor device structure, e.g. photovoltaic cell, has **semiconductor layer** which formed between pair of buffer **layers** on **polymer substrate**
Patent Assignee: WALPITA L M (WALP-I)
Inventor: WALPITA L M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6236061	B1	20010522	US 99227467	A	19990108	200149	B

Priority Applications (No Type Date): US 99227467 A 19990108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6236061	B1		9	H01L-029/78	

Abstract (Basic): US 6236061 B1
Abstract (Basic):
NOVELTY - A **semiconductor** (10) is sandwiched between a pair of buffer **layers**, which are formed on a **polymer substrate** (12). The **substrate** includes particulate filler for reducing the **coefficient** of thermal **expansion** (CTE) of the **polymer** to less than 40 ppm/degrees C.
USE - In e.g. light detectors, light emitting diodes (LED), thin **film** transistors (TFT), CMOSs, SRAMs, photovoltaic cells or solar cells.
ADVANTAGE - Improves **film** integrity without cracks.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the electronic device.
Semiconductor (10)
Polymer substrate (12)
pp; 9 DwgNo 1/6

39/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013940216
WPI Acc No: 2001-424430/200145
XRAM Acc No: C01-128380
XRPX Acc No: N01-314806

Contact structure for establishing electrical connection with contact targets, e.g. contact pads of electronic devices, has contactors formed on the **substrate** through microfabrication process

Patent Assignee: ADVANTEST KK (ADVA-N)
Inventor: FRAME J W; KHOURY T A

Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6250933	B1	20010626	US 2000488661	A	20000120	200145	B
DE 10101538	A1	20010802	DE 1001538	A	20010115	200145	
JP 2001284421	A	20011012	JP 200144302	A	20010117	200176	
KR 2001076422	A	20010811	KR 20013401	A	20010120	200213	

Priority Applications (No Type Date): US 2000488661 A 20000120
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6250933	B1		25	H01R-012/00	
DE 10101538	A1			G01R-031/28	
JP 2001284421	A		17	H01L-021/66	
KR 2001076422	A			H01R-012/00	

Abstract (Basic): US 6250933 B1
Abstract (Basic):

NOVELTY - A contact structure includes dielectric **substrate** (20) with depression, and contactors (30) having a bridge like shape formed on the **substrate** through a microfabrication process. The contactors are formed with a horizontal portion that produces a contact force when the contactor is pressed against a contact target.

DETAILED DESCRIPTION - A contact structure includes dielectric **substrate** with a depression, and contactors having a bridge like shape formed on the **substrate** through a microfabrication process. The contactors are formed with a horizontal portion having two angled portions connected to the dielectric **substrate**. The horizontal portion has a free end positioned over the depression on the dielectric **substrate**. The horizontal portion of the contactor produces a contact force when the contactor is pressed against a contact target such that the horizontal portion enters the depression while exerting the contact force.

USE - The contact structure is for establishing electrical connection with contact targets such as contact pads or leads of electronic circuits or devices. It is also used in integrated circuit packaging. It is particularly to be used in a probe card to test **semiconductor** wafers, **semiconductor** chips, packaged **semiconductor devices**, module sockets, printed circuit boards.

ADVANTAGE - The contact structure has a very high frequency bandwidth to meet the test requirements of next generation **semiconductor** technology. Since the contact structure is formed through a modern miniaturization technology, a large number of contactors can be aligned in a small space which is suitable for testing a large number of **semiconductor devices** at the same time. With the use of miniaturization technology without involving manual handling, it is possible to achieve consistent quality, high reliability and long life in the contact performance. Further, because the contactors can be fabricated on the same **substrate** material as that of the device under test, it is possible to compensate the temperature **expansion coefficient** of the device under test, which is able to avoid positional errors.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional diagram of a contact structure.

Substrate (20)

Contactors (30)

pp; 25 DwgNo 5/20

39/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013726396
WPI Acc No: 2001-210626/200121
Related WPI Acc No: 2002-224763
XRAM Acc No: C01-062503
XRPX Acc No: N01-150481

Creation of high density **semiconductor device** package involves mask less exposure to form interconnect **layers** on dielectric surface on metal **substrate**

Patent Assignee: THIN FILM MODULE INC (THIN-N)
Inventor: HO C W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6197614	B1	20010306	US 99467120	A	19991220	200121	B

Priority Applications (No Type Date): US 99467120 A 19991220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6197614	B1		10	H01L-021/44	

Abstract (Basic): US 6197614 B1
Abstract (Basic):

NOVELTY - Creation of a package for high density **semiconductor devices** comprises depositing an interconnect **layer** using maskless exposure equipment including plating and wet etch steps over the surface of a dielectric **layer** which is deposited over a surface of a metal **substrate**.

DETAILED DESCRIPTION - Creation of a package for high density **semiconductor devices** comprises cleaning first surface (24) of metal **substrate** (14) which also includes a second surface (26). A first **layer** of dielectric is deposited over the first surface. An interconnect **layer** is deposited over the surface of dielectric **layer** using maskless exposure equipment including plating and wet etch steps. A first **layer** of an interconnect **substrate** (12) having first and second surfaces is formed. The second surface of this interconnect **substrate layer** abuts to the first surface of the metal **substrate**. The interconnect **layer** (18) is deposited with a dielectric while further using a laser to create a via pattern through the dielectric to provide connections to an overlying interconnect **layer**. The deposition and **coating** steps are repeated for a multilayer structure. The last interconnect **layer** (20) of the interconnect **substrate** is **coated** with a dielectric as a solder mask. Metal pads within the first surface of the interconnect **substrate** are exposed to create openings for electrical connections. The second surface of the metal **substrate** is masked and etched to create opening(s) (28) to expose further portions of the dielectric within the openings. Openings are selectively created in the exposed dielectric and in the second surface of the interconnect **substrate** to provide points of

electrical access to the second surface of the interconnect **substrate**. The metal **substrate** is subdivided into individual integrated circuit chip (16) **substrates** or interconnect cards.

USE - For creating package for high-density **semiconductor devices**.

ADVANTAGE - The method provides a low-cost fabrication approach for prototype packaging **substrates** with a fast turn around time. It handles many different part types of **substrates** with different batch sizes in a most efficient manner and reduces performance limitations imposed by prior art high-density **semiconductor** manufacturing packaging techniques. It also eliminates the use of masks in processing the **substrates**, thus reducing the cost and improving the yield and reducing the material handling and throughput time. The invention provides for high pin fan-out for high density **semiconductor devices** and for device package that is devoid of warpage and dimensional variations during high temperature or wet chemical processing. The thermal **coefficient** of **expansion** of the dielectric **layer** is higher than that of the metal **substrate** and the **film** in the bottom of the opening is under tension and stretched taut. This **film** also absorbs little water, making it a stable surface that does not sag or deform.

DESCRIPTION OF DRAWING(S) - The figure shows a single chip wire bond chip package with two interconnect **layers**.

interconnect **substrate** (12)
metal **substrate** (14)
IC chip (16)
interconnect **layer** (18)
interconnect **layer** (20)
first surface (24)
second surface (26)
opening (28)
pp; 10 DwgNo 1/2

39/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013655687
WPI Acc No: 2001-139899/200115
XRAM Acc No: C01-041385
XRPX Acc No: N01-102014
Resin-sealed electronic device that mounts flip chip monolithic integrated circuit (IC) on hybrid circuit board through bumps
Patent Assignee: HITACHI CAR ENG CO LTD (HITA-N); HITACHI LTD (HITA); HITACHI CAR ELECTRONICS KK (HITA-N)
Inventor: FUKATSU K; KAMINAGA T; KOBAYASHI R; SHIDA M; SUGIURA N
Number of Countries: 027 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1043771	A2	20001011	EP 2000107061	A	20000404	200115	B
JP 2000294692	A	20001020	JP 9999088	A	19990406	200115	
US 6321734	B1	20011127	US 2000544555	A	20000406	200175	

Priority Applications (No Type Date): JP 9999088 A 19990406
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1043771	A2	E	22	H01L-023/29	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
JP 2000294692	A		12	H01L-023/29	
US 6321734	B1			H01L-023/29	

Abstract (Basic): EP 1043771 A2
Abstract (Basic):
NOVELTY - The device is packaged with a thermosetting **resin** (4) by transfer molding. The **resin** has a linear **expansion coefficient** of 3x10-6 to 17x10-6. It contains a filler having a particle size smaller than the height of the bump (2) by more than 10 microns.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for:
(1) a **resin** sealed electronic device where the bump is restrained from moving by transfer molding **resin** flowing around the transfer molding;
(2) a **resin** sealed electronic device where the gap between the flip chip type monolithic IC (1) and the hybrid circuit board (3) is filled with transfer molding **resin** (4) flown around during transfer molding excluding or including voids; and
(3) the fabrication of a **resin** sealed electronic device by molding using the transfer molding **resin** and applying a transfer molding pressure so the **resin** flows between the flip chip monolithic IC and the hybrid circuit board.
USE - Used for ignition coil for internal combustion (IC) engine.
ADVANTAGE - High reliability.
DESCRIPTION OF DRAWING(S) - The drawing shows a vertical cross-section of the **resin**-sealed electronic device.
Flip chip type IC (1)

Solder bump (2)
Hybrid circuit board (3)
Transfer molding **resin** (4)
Terminals (5)
Aluminum wire (6)
Pad (7)
pp; 22 DwgNo 1/16

39/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013177475
WPI Acc No: 2000-349348/200030
XRAM Acc No: C00-106111
XRPX Acc No: N00-261713
Chip carrier for use with one or more integrated circuits (ICs) having peripheral bond pads, has silicon **substrate**, electrically conducting vias, and patterned metal interconnections
Patent Assignee: SANDIA CORP (SAND-N)
Inventor: CHU D; GASSMAN R A; PALMER D W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6052287	A	20000418	US 97987276	A	19971209	200030	B

Priority Applications (No Type Date): US 97987276 A 19971209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6052287	A		8	H05K-007/02	

Abstract (Basic): US 6052287 A
Abstract (Basic):
NOVELTY - A chip carrier for use with one or more integrated circuits (ICs) having peripheral bond pads has silicon **substrate**; electrically conducting vias through the **substrate** in an array; and patterned metal interconnections on the lower **substrate** surface to have an electrical interconnection between the IC bond pads and the vias.

DETAILED DESCRIPTION - A chip carrier (10) for use with one or more integrated circuits (ICs) (100) having peripheral bond pads (102) comprises a) silicon **substrate**; b) electrically conducting vias (24) formed through the **substrate** in an array; and c) patterned metal interconnections formed on the lower **substrate** surface (16) to provide an electrical interconnection between the IC bond pads and the vias. The chip carrier is adapted to be mechanically and electrically bonded to each IC, so that the peripheral bond pads of each IC are electrically reconfigured.

USE - For use in ICs.

ADVANTAGE - The invention provides an interconnect re-routing structure on a crystalline **semiconductor substrate**, rather than relying plastic, ceramic or other non-**semiconductor** materials on which it is difficult to apply fine-line electrical interconnections, and which can be thermally disadvantageous. The same processes used for fabricating ICs can also be used for manufacturing the chip carrier, where it is formed from a silicon **substrate**, thus reducing cost and increasing manufacturing compatibility. It serves as an additional heat sink or heat spreader, and in particular as a thermal stress absorber when an IC chip is to be interfaced with a material, e.g. glass **epoxy** printed circuit board, a ceramic package or **aluminum/copper** plates which have high thermal

coefficients of **expansion,** thus creating a thermal-mechanical load on electrical interconnections to the IC. The re-routing of the IC die peripheral bond pads can alleviate problem of thermal-mechanical stress an d prevent potential failures of the electrical interconnections. It allows the use of standard commercial ICs to form a custom or high-performance circuit assembly. It also provides an inexpensive way to achieve a modification to a conventional IC without the need for changes to the original IC product.

DESCRIPTION OF DRAWING(S) - The figure shows a side elevation view of the chip carrier in conjunction with an integrated circuit chip.

Chip carrier (10)
Lower surface (16)
Solder ball (22)
Electrically conducting vias (24)
Integrated circuits (100)
Bond pads (102)
pp; 8 DwgNo 1/3

39/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012893351
WPI Acc No: 2000-065186/200006
XRPX Acc No: N00-051130
Structural mounting of **semiconductor device**
Patent Assignee: NEC CORP (NIDE); MORI F (MORI-I)
Inventor: MORI F
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2779867	A1	19991217	FR 997262	A	19990609	200006	B
JP 11354677	A	19991224	JP 98161646	A	19980610	200011	
JP 3070579	B2	20000731	JP 98161646	A	19980610	200041	
US 20010040791	A1	20011115	US 99328894	A	19990609	200172	

Priority Applications (No Type Date): JP 98161646 A 19980610
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2779867	A1		29	H01L-021/58	
JP 11354677	A		9	H01L-023/12	
JP 3070579	B2		8	H01L-023/12	Previous Publ. patent JP 11354677
US 20010040791	A1			H01L-021/44	

Abstract (Basic): FR 2779867 A1
Abstract (Basic):
NOVELTY - The method of mounting includes the bonding of the upper surface of **semiconductor** (30) to a plate (50), the positioning so that the input/output terminals (31) are opposite to plots (11) on a printed **substrate** (10) with intermediate connecting elements (20), the melting of the connecting elements by heating, and cooling to normal temperature. The **coefficient** of thermal **expansion** of the plate is close or equal to that of the **substrate**, and the bonding of the **semiconductor** becomes a function of that of the plate.
DETAILED DESCRIPTION - The **semiconductor device** is an integrated circuit (IC), or a large-scale integration (LSI) implementation. The plate (50) is metallic, made of e.g. **copper** or brass, and the connecting elements are balls of solder. The **adhesive** is of **epoxy** type, and is applied in a **layer** of thickness 10-20 micrometers. An organic **substrate** can be used instead of the metallic plate, as well as the printed **substrate**. In the case of ceramic **substrate**, the plate is made of **aluminum** nitride, or ceramic compounds of **aluminum** or tungsten, and a conducting **adhesive** is used instead of solder. The plate can be in the form of a lid enclosing the **semiconductor** . The mounting can include a heat-dissipating element fastened by screws to the metallic plate.
USE - In fabrication of **semiconductor devices**, in particular in mounting of flip chips.
ADVANTAGE - Improved reliability of **semiconductor**

devices, due to compensation of different rates of thermal expansion.

DESCRIPTION OF DRAWING(S) - The drawing is a cross-sectional view of the structural mounting.

Substrate (10)
Plots (11)
Connecting elements (20)
Semiconductor (30)
Terminals (31)
Layer of **adhesive** (40)
Plate (50)
pp; 29 DwgNo 1/6

39/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012401117
WPI Acc No: 1999-207224/199918
Related WPI Acc No: 2002-293981
XRAM Acc No: C99-060563
XRPX Acc No: N99-152738
Semiconductor package in which the **semiconductor** chip is bonded into
Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: HIRANO K; NAKATANI S
Number of Countries: 030 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 907205	A2	19990407	EP 98119039	A	19981002	199918 B
CN 1214545	A	19990421	CN 98124628	A	19980930	199934
JP 11168112	A	19990622	JP 98262873	A	19980917	199935
KR 99036866	A	19990525	KR 9841676	A	19981002	200032
TW 407353	A	20001001	TW 98115960	A	19980925	200132
US 6300686	B1	20011009	US 98158299	A	19980922	200162
US 20020028536	A1	20020307	US 98158299	A	19980922	200221
			US 2001927164	A	20010810	
KR 297915	B	20010807	KR 9841676	A	19981002	200227

Priority Applications (No Type Date): JP 97270006 A 19971002
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 907205	A2	E	25	H01L-021/56	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
CN 1214545	A			H01L-023/28	
JP 11168112	A		14	H01L-021/56	
KR 99036866	A			H01L-023/48	
TW 407353	A			H01L-023/08	
US 6300686	B1			H01L-023/48	
US 20020028536	A1			H01L-021/44	Div ex application US 98158299 Div ex patent US 6300686
KR 297915	B			H01L-023/48	Previous Publ. patent KR 99036866

Abstract (Basic): EP 907205 A2
Abstract (Basic):
NOVELTY - A **semiconductor** package is formed by bonding the electrode surface and edges of a **semiconductor** chip to a thermal conductive material containing 70-95 pts.wt. inorganic filler and 5-30 pts.wt. thermosetting **resin** composition and electrically connecting the electrode surface with an external lead electrode.
DETAILED DESCRIPTION - Holes are made in a sheet of the thermally conductive material and filled or partially filled with a conductive **resin** composition. When the chip and thermally conductive

material are pressed together bumps formed on the electrodes of the chip penetrate the holes and make electrical contact with the conductive **resin** filling. Lead electrodes are connected to the other end of the **resin** filled hole or, alternatively, a wiring **substrate** of the same thermally conductive material containing preplaced electrodes is pressed onto the package so that one set of electrodes contacts the chip via the conductive **resin** and the other set forms the lead electrodes. An INDEPENDENT CLAIM is included for the method of manufacture of the **semiconductor** package including the simultaneous manufacture of a number of packages which are then divided.

USE - The **semiconductor** package is used for miniaturized electronic devices.

ADVANTAGE - As compared with the chip scale package (CSP) package the proposed package has improved thermal conductivity between the chip and the wiring **substrate** which prevents heat build up and better resistance to thermal shock because the thermal **expansion coefficients** of the chip package and **substrate** are the same. There is no requirement for the use of sealing **resin** to ensure air tightness. This reduces the complexity and cost of manufacture.

DESCRIPTION OF DRAWING(S) - The drawing shows the steps in the manufacturing process.

thermal conductive sheet (31)
mold release **layer** (32)
through hole (33)
conductive **resin** (34)
semiconductor chip (35)
external lead electrode (36)
thermal conductive mixture after pressing. (37)
pp; 25 DwgNo 3/10

39/3,AB/14 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

06754854
POWER **SEMICONDUCTOR DEVICE**

PUB. NO.: 2000-340719 [JP 2000340719 A]
PUBLISHED: December 08, 2000 (20001208)
INVENTOR(s): KUSHIMA TADAO
TANAKA AKIRA
SAITO RYUICHI
SUZUKI KAZUHIRO
KOIKE YOSHIHIKO
SHIMIZU HIDEO
APPLICANT(s): HITACHI LTD
APPL. NO.: 11-145973 [JP 99145973]
FILED: May 26, 1999 (19990526)

ABSTRACT

PROBLEM TO BE SOLVED: To improve a level of insulating withstand voltage by **coating** a boundary of a conductive part on a creepage surface of an insulating **substrate** between a conductive pattern end and a base plate with an amorphous inorganic glass material, which is larger in breakdown voltage than an insulation-resistant gelling agent and has high resistance against discharged withstand voltage.

SOLUTION: A boundary of the end of a conductive pattern 3b is **coated** on the creepage surface of an insulating **substrate**, such as **aluminum** nitride 3a. The conductive patterns 3b, such as **Cu** foil, are brazed with Ag on both surfaces of the insulating **substrate**. For instance, a discharging method such as a mask printing method is used. **Coating** is made with crystalline inorganic glass 4a such as a Bi2O3-B2O3 material, which is higher in breakdown voltage than an insulation-resistant gelling agent 5a by 10 kV or higher, has high resistance against discharged withstand voltage, and has a thermal **expansion coefficient** of 3.2 to 12.5×10-6/°C. Afterwards, a heating operation is performed in the air or in N2 gas, and fusion bonding is carried out at a sealing temperature of 410 to 750°C. A case structure 6, which is made of a polyphenylene sulfide insulating **resin** material, is bonded and sealed into the peripheral part of a base plate 1 with an **adhesive** 7 made of silicon **resin**, to complete a module.

39/3,AB/15 (Item 15 from file: 347)
DIALOG(R)File 347:JAPIO

06413029
SEMICONDUCTOR DEVICE

PUB. NO.: 11-354687 [JP 11354687 A]
PUBLISHED: December 24, 1999 (19991224)
INVENTOR(s): KURIHARA YASUTOSHI
ENDO TSUNEO
IIZUKA MAMORU
KOYAMA KENJI
NIITSU TOSHIJI
APPLICANT(s): HITACHI LTD
APPL. NO.: 10-164679 [JP 98164679]
FILED: June 12, 1998 (19980612)

ABSTRACT

PROBLEM TO BE SOLVED: To prevent thermal fatigue breakdown of a soldering part due to the difference in thermal **expansion coefficients**, when **resin** molding is made after a component is fixed on a **semiconductor substrate** by soldering.

SOLUTION: In an insulating board 10, a **copper** wiring **layer** 3 is selectively formed on a main surface of an **aluminum** plate 1 as the base material, via an **epoxy** insulating **resin layer** 2. On the insulating board 10, a **semiconductor** element **substrate** 21, a passive element composed of a chip resistor 22 and a chip capacitor 23, a terminal 24 are fixed by alloy materials 25, 25', in which one or more kinds of metals selected from among Sb, Ag, Zn, In, Bi and **Cu** are added to Sn as the main component. A heat dispersing member 27 is arranged between the insulating board 10 and the **semiconductor substrate** 21. An **Al** wire (diameter: 300 μm) 26 is formed between the **substrate** 21 and the **copper** wiring **layer** 3 by ultrasonic bonding. Through potting method, the mounting part of the **substrate** 21 and a passive element is covered with **epoxy resin**, whose thermal **expansion coefficient** is adjusted to be 13-21 ppm/°C. The **epoxy resin** 31 id covered with silicone gel **resin** 32. A **resin** case 33 serving as an envelope is formed around a structure of such a constitution.

L31 ANSWER 21 OF 24 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:562153 HCAPLUS
DN 121:162153
TI Lead frames having improved surface and their manufacture
IN Matsunaga, Hideki; Oomori, Hirofumi; Nakamura, Shinichi; Ishii, Kimiko; Yamashita, Tsutomu; Endo, Hiroshi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06025776	A2	19940201	JP 1992-179509	19920707

AB The frames have **substrates** consisting of **Cu**-(5-95%)Fe alloys with or without Cr 0.1-20, Ni 0.1-10, **Al** 0.01-0.3, Ti 0.001-3, V 0.001-1, Nb 0.01-1, Zr 0.001-1, Mg 0.01-1, Si 0.01-1, Mn 0.01-1, P 0.01-1, Zn 0.01-1, and/or B 0.0005-1%; surface parts covering the **substrates**; c/c' >1 (c' = **Cu** concn. in the **substrates**, c = **Cu** concn. in the surface parts); and contain 0.02-10 ppm in total of anions, alkali metals, and/or org. acids, and the top surface of the surface parts is **coated** with 10-500 .ANG. **Cu** oxide **film**. The frames are manufd. by pickling surface of lead frame moldings and washing them with hot water. The lead frames have high reliability in working, i.e., mounting, bonding, **coating**, **soldering**, etc.

L31 ANSWER 22 OF 24 HCAPLUS COPYRIGHT 2002 ACS
AN 1979:621352 HCAPLUS
DN 91:221352
TI Solder for **semiconductor device** fabrication
IN Tanii, Takanobu; Yokozawa, Masami; Mizukoshi, Kanji
PA Matsushita Electronics Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 54062949	A2	19790521	JP 1977-130057	19771028

AB A solder used to join a **semiconductor substrate** to a **substrate** holder is prepd. by **coating** a Pb-Sn alloy or alloy contg. Pb and Sn as the principal constituent(s) with a thin **film** (0.01-0.03 .mu. of a metal (e.g. Au, Ag, **Cu**, Rh) whose ionization potential is lower than that of the solder metals. The solder surface can be kept clean during soldering, the surface tension of the **molten** solder can be lowered, the attraction of the **molten** solder to the **semiconductor substrate** and holder becomes uniform, and the solder thickness at the joint becomes uniform and free of hollows.

L31 ANSWER 23 OF 24 HCAPLUS COPYRIGHT 2002 ACS
AN 1975:420799 HCAPLUS
DN 83:20799
TI Soft-soldering contact in **semiconductor device**
IN Woelfle, Rudolf; Deyl, Vladimir
PA Siemens A.-G., Ger.
SO Ger. Offen., 13 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI DE 2340423	A1	19750220	DE 1973-2340423	19730809

AB **Al** contacts are made solderable by intermediate, metallic bonding **layers**. Thus, the **Al layer**, 2-10 .mu.m thick, on the top side of the **substrate**, is etched, plated chem. with 1.mu.m Ni contg. 1-10% **Cu**, and solder applied contg. 3-6% Sn. An alternate process applies 0.1 .mu.m Au over the Ni before the solder. The other side of the **substrate** is **coated** first with Ni silicide, then Ni, and finally with solder.

L31 ANSWER 24 OF 24 HCAPLUS COPYRIGHT 2002 ACS
AN 1970:524944 HCAPLUS
DN 73:124944
TI Forming an electrically-conductive connection on an electronic device
PA Philips Electronic and Associated Industries Ltd.
SO Brit., 4 pp.
CODEN: BRXXAA
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI GB 1204263		19700903		
PRAI NL		19670125		

AB A method is described for forming an elec. conductive connection on a surface portion of an electronic device. E.g., a **layer** of Si oxide is formed on an n-type Si wafer and an opening is formed in the **layer**. By diffusion, the region below the opening is converted to p-type. A further oxide **layer** forms in the opening and on the existing oxide **layer**. By masking and etching, 2 openings are provided in the oxide **layers** to expose the p-type Si and the original n-type **substrate**. A **layer** of Ag and then a **layer** of **Al** are deposited over the surface. The **Al layer** is **coated** with a photosensitive mask in which 2 apertures are provided. The body is transferred to an etching bath until the free **Al** in the apertures is dissolved and then to an electroplating bath. At a suitable temp. and a voltage of 1/5 V, 2 **Cu** connections are deposited on the exposed portions of the Ag **layer** at the openings. The masking **layer** is removed. The upper surface of the wafer with the exception of the connections consists of **Al**. By dipping in a **molten** solder (60Sn-40Pb) at 300.degree., the connections are covered with **solder layers**; the **Al** is not wetted by the solder. The remaining **Al layer** is removed with an etching soln. The exposed parts of the **Al layer** are dissolved by acid soln. The resultant structure of the body has 2 upper connections with **solder coatings**.

L37 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:37275 HCAPLUS
DN 124:132457
TI H2O enhanced focused ion beam micromachining
AU Stark, T. J.; Shedd, G. M.; Vitarelli, J.; Griffis, D. P.; Russell, P. E.
CS North Carolina State Univ., Raleigh, NC, 27695, USA
SO Journal of Vacuum Science & Technology, B: Microelectronics and Nanometer Structures (1995), 13(6), 2565-9
CODEN: JVTBD9; ISSN: 0734-211X
PB American Institute of Physics
DT Journal
LA English
AB The use of H2O vapor as a chem. adjunct for focused ion beam micromachining was studied. The presence of H2O vapor during micromachining with a 25 keV Ga+ beam increases the removal rate of carbon-contg. materials such as **polyimide**, PMMA, and other resists by a factor of 20 (relative to phys. sputtering), and that of diamond by a factor of 10. H2O causes a decrease in the removal rate of some other materials (e.g., Si and **Al**) by as much as a factor of 10, effectively increasing the selectivity of **polymers** over these other materials by as much as a factor of 200. The dependence of the removal rate on H2O pressure at the sample, pixel dwell time, pixel size, pattern **frame** time (corresponding to pattern size), and c.d. was studied using PMMA. PMMA removal rates were calcd. by measuring the depth of **rectangular** pits micromachined into PMMA films under the various exptl. conditions. In addn. to studying the effect of H2O on material removal rates, the change in removal rate of PMMA in the presence of selected gases including O2, H2, and CH3OH, was measured.

39/3,AB/16 (Item 16 from file: 347)
DIALOG(R)File 347:JAPIO

04335043
INSULATED HEAT DISSIPATING **SUBSTRATE** FOR **SEMICONDUCTOR** ELEMENT MOUNTING

PUB. NO.: 05-326743 [JP 5326743 A]
PUBLISHED: December 10, 1993 (19931210)
INVENTOR(s): KAWAMOTO KENICHIRO
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-151427 [JP 92151427]
FILED: May 19, 1992 (19920519)
JOURNAL: Section: E, Section No. 1520, Vol. 18, No. 141, Pg. 156, March 09, 1994 (19940309)

ABSTRACT

PURPOSE: To realize an insulated heat dissipating **substrate** for **semiconductor** element mounting use, which has a thermal **expansion coefficient** approximate to those of a **semiconductor** element to be mounted and an enclosure material, is superior in heat conductivity so as to be able to dissipate efficiently heat, which is generated from the element, and at the same time, is provided with electrical insulation properties.

CONSTITUTION: An insulated heat dissipating **substrate** 4 for mounting a **semiconductor** element 9 consists of a **substrate** main body 1 made of a **Cu**-W, **Cu**-Mo or **Al**-Si composite alloy and a heat-resistant organic insulator **film** 3 provided on the surface of the **substrate** main body 1, the **film** 3 contains 60 to 90 wt. % of diamond, cubic crystal boron nitride or **aluminium** nitride powder as a heat conductive filler and the **film** thickness of the **film** 3 is 10 to 60.mu.m.

39/3,AB/17 (Item 17 from file: 347)
DIALOG(R)File 347:JAPIO

03842155
IMAGE SENSOR AND IMAGE SENSOR UNIT

PUB. NO.: 04-207255 [JP 4207255 A]
PUBLISHED: July 29, 1992 (19920729)
INVENTOR(s): NAKAMURA TETSURO
TANAKA EIICHIRO
FUJIWARA SHINJI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-332431 [JP 90332431]
FILED: November 28, 1990 (19901128)
JOURNAL: Section: E, Section No. 1290, Vol. 16, No. 542, Pg. 147, November 12, 1992 (19921112)

ABSTRACT

PURPOSE: To inexpensively form the image sensor by packaging the image sensor on a light transparent **substrate** provided with circuit conductors without using wirings consisting of fine metallic wires and without forming bump electrodes on **semiconductor** elements.

CONSTITUTION: Photodetectors 17 and access circuits are provided on an Si **substrate**. The respective electrodes 14 are formed of 2 **layers** of **Al** wirings to about several .mu.m thickness from the **substrate** surface. The **substrate** is cut to form chips 13. The circuit conductor **layer** 12 consisting of **Cu**, etc., is formed on the light transparent **substrate** 11. A transparent curing type **resin** 15 is printed and applied in a prescribed amount on the prescribed position of the light transparent **substrate** 11. While the chip 13 is pressurized from above, the transparent curing type **resin** 15 is irradiated with UV rays through the light transparent **substrate** 11 and is thereby cured. The surface is **coated** with a protective **layer** 16 to complete the image sensor. The thickness, transmittance, shrinkage rate on heating and **coefficient** of thermal **expansion** of the light transparent **substrate** are selected respectively within specified ranges at this time. The chip is irradiated from the **semiconductor** element side and the other surface is used as a surface for tight contact with originals. The light is introduced through the light transparent **substrate** 11 to the photodetector 7. The high-performance image sensor is obtained according to this constitution.

39/3,AB/18 (Item 18 from file: 347)
DIALOG(R)File 347:JAPIO

03797656
SEMICONDUCTOR MODULE

PUB. NO.: 04-162756 [JP 4162756 A]
PUBLISHED: June 08, 1992 (19920608)
INVENTOR(s): SATO HIDEKI
KOMORIDA YUTAKA
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-289781 [JP 90289781]
FILED: October 26, 1990 (19901026)
JOURNAL: Section: E, Section No. 1269, Vol. 16, No. 462, Pg. 46, September 25, 1992 (19920925)

ABSTRACT

PURPOSE: To enhance the heat cycle characteristics by relieving a thermal stress caused by the difference in the **coefficient** of thermal **expansion** between a **copper layer** and a heat sink by bonding an **aluminum** nitride **substrate** to the heat sink with an organic-based heat-resistant **adhesive** through a **copper layer** directly bonded to the **aluminum** nitride **substrate**.

CONSTITUTION: **Copper layers** 2 and 3 are respectively bonded directly to both the main faces of an **aluminum** nitride **substrate** 1, and the **copper layer** 2 is used for mounting a **semiconductor** and has a required circuit pattern. Also the **copper layer** 3 becomes the junction with a heat sink. A **semiconductor device** 5 is bonded with a solder **layer** 6 and a **semiconductor device** 5 is mounted on the **copper layer** 2 at the mounting side, and the **semiconductor device** 5 is electrically connected to the circuit of the **copper layer** at the mounting side with bonding wires 7 and others. Also, the **copper layer** at the bonding side is bonded to a heat radiating container 8 functioning as a heat sink with an organic-based heat-resistant **adhesive** 9. By doing this, the thermal stress due to the difference in the **coefficient** of thermal **expansion** between the **copper layer** and heat sink can be relieved and the heat cycle characteristics can be enhanced.

39/3,AB/19 (Item 19 from file: 347)
DIALOG(R)File 347:JAPIO

03751860
SEMICONDUCTOR CIRCUIT **DEVICE**

PUB. NO.: 04-116960 [JP 4116960 A]
PUBLISHED: April 17, 1992 (19920417)
INVENTOR(s): KATO HAJIME
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-237926 [JP 90237926]
FILED: September 07, 1990 (19900907)
JOURNAL: Section: E, Section No. 1245, Vol. 16, No. 367, Pg. 55, August 07, 1992 (19920807)

ABSTRACT

PURPOSE: To inhibit the generation of a thermal stress and the temperature rise of a **semiconductor** element by a method wherein in the case the element is mounted on an insulating circuit board via a heat sink, a composite material consisting of **copper** and glass is used as the material for the heat sink.

CONSTITUTION: An insulating circuit board 5 is bonded on a heat sink 7 made of **Al** through a silicon **resin** adhesion **layer** 6 and a heat sink 9 made of a molybdenum and a power transistor chip 1 are soldered in order on the **substrate** 5. In this constitution, a composite material consisting of **copper** and glass is used as the material for the sink 9. This composite material is obtained by a method wherein **copper** powder and glass are kneaded so that the content of **copper** becomes 90wt.% to form into a pasty form, the pasty material is flowed in a metal mold and the powder and the glass are integrally sintered at 800 deg.C. Thereby, heat, which is generated when the chip 1 is actuated, is effectively dissipated. Moreover, a difference between the linear **expansion coefficients** of the sink 9 and the **substrate** 5 is small and no crack is generated in solder **layers** 2 and 4.

39/3,AB/20 (Item 20 from file: 347)
DIALOG(R)File 347:JAPIO

03359537
MANUFACTURE OF **SEMICONDUCTOR DEVICE**

PUB. NO.: 03-022437 [JP 3022437 A]
PUBLISHED: January 30, 1991 (19910130)
INVENTOR(s): MORIYAMA YOSHIFUMI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-157692 [JP 89157692]
FILED: June 19, 1989 (19890619)
JOURNAL: Section: E, Section No. 1055, Vol. 15, No. 147, Pg. 46, April 12, 1991 (19910412)

ABSTRACT

PURPOSE: To absorb stress generated due to thermal **expansion coefficient** difference between an element and a mounting **substrate**, and to reduce defective opening by forming a metallic **layer** burying an opening section through a plating method by utilizing a mask shaped onto a barrier metallic **layer**, **coating** the metallic **layer** with a high-temperature **resin** in the thickness of approximately half the thickness of the metallic **layer**, exposing the top face and side face of the upper half of the metallic **layer** and forming a solder bump electrode through a solder dipping method.

CONSTITUTION: An **Al** electrode 3 is shaped onto a silicon **substrate** 1, the periphery of the **Al** electrode 3 is protected by an insulating **film** 2, and a barrier metallic **layer** 4 is formed onto the whole surface. A resist 5 is shaped onto the barrier metallic **layer** 4, and an opening section is formed onto the **Al** electrode 3 as an exposure phenomenon. A metallic **layer** such as a **Cu layer** 6 is shaped through metallic plating while using the barrier metallic **layer** 4 as an electrode. The resist is removed, the barrier metallic **layer** 4 in the periphery of the electrode is removed through etching, and a **Cu** columnar electrode is formed onto the **Al** electrode 3 while employing **Cu** as an etchant. A high-temperature **resin film** such as a **polyimide film** 7 is shaped in thickness thinner than a periphery on the **Cu layer** 6, and the **polyimide film** on the surface of the **Cu layer** 6 is removed and the **polyimide film** in the periphery of the **Cu layer** 6 is left through dry etching. A solder electrode 8 is formed to the upper section of the **Cu layer** 6 through solder dipping.

39/3,AB/21 (Item 21 from file: 347)
DIALOG(R)File 347:JAPIO

03140697
MULTILAYER WIRING BOARD FOR **SEMICONDUCTOR** PACKAGING

PUB. NO.: 02-116197 [JP 2116197 A]
PUBLISHED: April 27, 1990 (19900427)
INVENTOR(s): NOZAKI TAKAYUKI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
HITACHI MICRO COMPUT ENG LTD [470864] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-268047 [JP 88268047]
FILED: October 26, 1988 (19881026)
JOURNAL: Section: E, Section No. 955, Vol. 14, No. 344, Pg. 25, July 25, 1990 (19900725)

ABSTRACT

PURPOSE: To prevent the warp of the title device due to heat by forming a composite **layer** consisting of materials having different thermal **expansion coefficients** inside a **substrate**.

CONSTITUTION: Both surface **layers** 1, 2 of a **substrate** 6 consist of a glass **epoxy** plate, etc. An intermediate **layer** 3 is composed of a composite **layer** which consists of materials having different thermal **expansion coefficients** . As a desirable example of the **layer** 3, a combination of large thermal **expansion coefficient** difference such as combination of **Al** and **Cu**, and Sn and Ni is recommended taking the balance of warp of the **substrate** 6, etc., into consideration. If the **layer** 3 is interposed in this way, characteristic to warp larger than temperature rise can be acquired based on the principle of bimetal. According to this characteristic, it becomes possible to make a **substrate** warp in the opposite direction to the warp of the **substrate** and to compensate for the warp amount of the **substrate** due to heat.

39/3,AB/22 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO

03062235
MOUNTING STRUCTURE OF **SEMICONDUCTOR** CHIP

PUB. NO.: 02-037735 [JP 2037735 A]
PUBLISHED: February 07, 1990 (19900207)
INVENTOR(s): YAMAZAKI SHUNPEI
OKA TAKESHI
MASE AKIRA
APPLICANT(s): SEMICONDUCTOR ENERGY LAB CO LTD [470730] (A Japanese Company or Corporation), JP (Japan)
OMRON TATEISI ELECTRON CO [000294] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-189316 [JP 88189316]
FILED: July 27, 1988 (19880727)
JOURNAL: Section: E, Section No. 918, Vol. 14, No. 190, Pg. 80, April 18, 1990 (19900418)

ABSTRACT

PURPOSE: To improve reliability against burnout due to thermal distortion by providing a substance whose thermal **coefficient** of **expansion** is larger than the solid state properties of a board and is smaller than that of a material constituting an electrical wiring between the **substrate** and the electrical wiring.

CONSTITUTION: A **film** 2 with the solid state properties between a thermal **coefficient** of **expansion** owned by a board 1 and that owned by an electrical wiring 3 is formed on the board 1 which has insulation properties on the surface and at least a wavelength of 320nm-400nm is formed. After that, the electrical wiring 3 is formed by the printing method with a paste including at least one type or more conductive metal grains among Fe, **Cu**, Ag, Pd-Ag, Pt, **Al**, C, Sn, In, Ni, Ta, Ti, Sb and Mo and metal, **copper**, or bump 4 consisting of solder are contacted mechanically at the upper part of the wiring and at least on the surface of a **semiconductor** chip. Thus, the board 1 and the **semiconductor** chip 5 are bonded by an **epoxy resin** 6 of ultraviolet-rays curing type. It improves reliability against burnout, etc., due to thermal distortion without increasing production cost.

39/3,AB/23 (Item 23 from file: 347)
DIALOG(R)File 347:JAPIO

02821472
MANUFACTURE OF FLEXIBLE PHOTOELECTRIC CONVERSION ELEMENT

PUB. NO.: 01-119072 [JP 1119072 A]
PUBLISHED: May 11, 1989 (19890511)
INVENTOR(s): TSUNOHASHI TAKESHI
GOTO KAZUHITO
NAMIKAWA AKIRA
TATSUMI MOTOSHIGE
APPLICANT(s): NITTO DENKO CORP [000396] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-277125 [JP 87277125]
FILED: October 31, 1987 (19871031)
JOURNAL: Section: E, Section No. 804, Vol. 13, No. 359, Pg. 103, August 10, 1989 (19890810)

ABSTRACT

PURPOSE: To reduce or eliminate heat shrinkage and to prevent generation of curl of a flexible photoelectric conversion element when temperature is cooled down to a room temperature by allowing an electrical insulation **layer** with nearly the same thermal **coefficient** of **expansion** as a transparent plastic **substrate** to join a **semiconductor layer** at high temperature through a rear surface electrode **layer**.

CONSTITUTION: A **film** is continuously formed by casting a solution of **polyimide** precursor to a support consisting of a roll-like **copper** box. A **semiconductor layer** with photoconductivity consisting of p-type-i-type-n-type amorphous silicon thin **film** is formed on an colorless and transparent **polyimide film substrate** through a conductive thin **film** of ITO. Then, it is retained within a high-vacuum metal deposition device and an **aluminum** rear surface electrode **layer** with a thickness of 0.1.mu.m is built up on an n-type amorphous silicon thin **film**. Then, an electrical insulation **layer** is formed by changing into imide and the support is eliminated by performing etching to obtain a flexible photoelectric conversion element consisting of a **substrate**, a transparent electrode **layer**, a **semiconductor layer**, a rear surface electrode, and an electrical insulation **layer** . The flexible photoelectric conversion element thus obtained is flat in terms of appearance and does not produce curl.

39/3,AB/24 (Item 24 from file: 347)
DIALOG(R)File 347:JAPIO

02707492
CIRCUIT **SUBSTRATE** FOR HIGH POWER AND HYBRID INTEGRATED CIRCUIT THEREOF

PUB. NO.: 01-005092 [JP 1005092 A]
PUBLISHED: January 10, 1989 (19890110)
INVENTOR(s): KATO KAZUO
NAKANO TATSUO
ASAI SHINICHIRO
APPLICANT(s): DENKI KAGAKU KOGYO KK [000329] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-161810 [JP 87161810]
FILED: June 29, 1987 (19870629)
JOURNAL: Section: E, Section No. 749, Vol. 13, No. 176, Pg. 9, April 25, 1989 (19890425)

ABSTRACT

PURPOSE: To stabilize the **adhesive** property and the dielectric strength property with respect to an insulating **layer** and a **copper** foil, and to prevent the insulating **layer** from cracking, by superposing an **Al** foil on the insulating **layer** of a metallic **substrate** and by forming a **copper** foil with wall thickness on the **Al** foil.

CONSTITUTION: A bonding pads 3 of **Al** foil etched are formed on an insulating **layer** 5 which is laminated on a metallic **substrate** 6 of **Al** or the like. And a **copper** foil **layer** 1 with wall thickness of more than 35.mu.m is laminated on each of the bonding posts 3. Moreover, a **semiconductor device** consisting of a power transistor 7 or the like is mounted on a part of the **copper** foil **layer** 1 with wall thickness through an eutectic solder 10. The transistor 7 is connected to other bonding post 3 through an **Al** wire 9. Therefore, the **adhesive** strength between the metallic foil **layer** and the insulating **layer** increases and being stabilized. Besides, the thermal stress resulting from the difference of **expansion coefficient** between the metallic **substrate** and the **copper** foil is reduced to prevent the insulating **layer** from being damaged without the dielectric strength being lowered.

39/3,AB/25 (Item 25 from file: 347)
DIALOG(R)File 347:JAPIO

02685626

SEMICONDUCTOR DEVICE

PUB. NO.: 63-302526 [JP 63302526 A]
PUBLISHED: December 09, 1988 (19881209)
INVENTOR(s): ADACHI TOSHINORI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-138496 [JP 87138496]
FILED: June 02, 1987 (19870602)
JOURNAL: Section: E, Section No. 738, Vol. 13, No. 139, Pg. 116, April 06, 1989 (19890406)

ABSTRACT

PURPOSE: To prevent the generation of defective insulation in a **semiconductor** base **substrate** by forming a first metallized **layer** consisting of a first metal having a thermal **expansion coefficient** approximating to that of an insulating heat-transfer **layer** to the upper section of the insulating **layer** and shaping a second metallized **layer** composed of a second metal having a thermal **expansion coefficient** smaller than that of the first metal onto the first metallized **layer**.

CONSTITUTION: An insulating **film** 2 is formed onto the surface of a **semiconductor** base **substrate** 1, a first metallized **layer** 3 made up of a first metal having a thermal **expansion coefficient** approximating to that of the insulating **layer** 2 is shaped to the upper section of the insulating **layer**, and a second metallized **layer** at consisting of a second metal having a thermal **expansion coefficient** smaller than that of the first metal is formed onto the first metallized **layer** 3. An insulating **substrate** in which the insulating **layer** 2 such as an insulating heat transfer **layer** 2 shaped by a high molecular **resin** containing inorganic powder and glass fiber is formed onto a heat-dissipating **substrate** 1 composed of **Al** and the first metallized **layer** 3 such as an **Al** electrode **layer** 3 and the second metallized **layer** 4 such as a **Cu** electrode **layer** 4 are metallized and shaped to the upper section of the **layer** 2 is employed as the **semiconductor** base **substrate**. Accordingly, the mechanical stress of the insulating **layer** due to the difference of the thermal **expansion coefficients** of each **layer** is reduced, thus minimizing defective insulation.

39/3,AB/26 (Item 26 from file: 347)
DIALOG(R)File 347:JAPIO

02543469
WIRING BOARD FOR MOUNTING **SEMICONDUCTOR** ELEMENT

PUB. NO.: 63-160369 [JP 63160369 A]
PUBLISHED: July 04, 1988 (19880704)
INVENTOR(s): KUWASHIMA HIDEJI
NAKANO NAOKI
APPLICANT(s): HITACHI CHEM CO LTD [000445] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-313781 [JP 86313781]
FILED: December 24, 1986 (19861224)
JOURNAL: Section: E, Section No. 680, Vol. 12, No. 423, Pg. 85, November 09, 1988 (19881109)

ABSTRACT

PURPOSE: To enhance the bonding strength and the airtightness by a method wherein a conductive circuit, a wire-bonding part and a small through hole, to be used for inserting and fixing a pin, are formed at parts, on a **substrate**, where a **semiconductor** element is not mounted and a heat-conducting plate is installed inside a big through hole in the central part of the **substrate** while the parts excluding the tip of the pin, the wire-bonding part and the heat- conducting plate are **coated** with a **synthetic resin**.

CONSTITUTION: A heat-conducting plate 8 is composed of a metal material, such as **copper**, **Al** or the like, whose heat conduction performance is excellent and whose **coefficient** of thermal **expansion** is close to that of a **semiconductor device**; a protruding part 9 is formed. A **substrate** is composed of a **resin** such as polyester or the like to which a sheet of **film**-like **copper** foil is glued. A small through hole 1 is made at a part other than the central part 6 of a **substrate** 5; a conductive circuit 2, an internal edge part 3 for a wire-bonding part, an external edge part 4 for this part and a big through hole 7 are formed by an etching method. Then, the protruding part 9 of the heat-conducting plate 8 is inserted into the big through hole 7 and a nailhead pin 11 is inserted into the small through hole 1; a prescribed part is **coated** with an **epoxy resin** composition 12. By this method, it is possible to obtain a wiring board whose mechanical strength, heat-radiating efficiency and airtightness are excellent and where a **semiconductor**-mounting part is provided on the upper face of a flat part 18 on the heat-conducting plate 8.

39/3,AB/27 (Item 27 from file: 347)
DIALOG(R)File 347:JAPIO

02287651

SUBSTRATE FOR **SEMICONDUCTOR DEVICE**

PUB. NO.: 62-204551 [JP 62204551 A]
PUBLISHED: September 09, 1987 (19870909)
INVENTOR(s): YAMANAKA SEISAKU
IHARA HIROHIKO
IGARASHI TADASHI
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-047798 [JP 8647798]
FILED: March 05, 1986 (19860305)
JOURNAL: Section: E, Section No. 585, Vol. 12, No. 63, Pg. 21, February 25, 1988 (19880225)

ABSTRACT

PURPOSE: To obtain the **substrate**, to be sued for **semiconductor device** and having excellent productivity, on which a plurality of large-sized elements can be mounted, by a method wherein a lead part for external connection formed separately and an element-mounting wiring **substrate**, consisting of the material having the thermal **expansion coefficient** of 10X10(sup -6)/ deg.C or less, are coupled and after elements have been mounted and an internal wiring has been finished, they are sealed with **resin** or glass.

CONSTITUTION: The material having the thermal **expansion coefficient** of 10X10(sup -6)/ deg.C or less such as 42-alloy and the like is sued as the material for a **substrate** 2, the insulative **film** 6 such as a metal oxide and the like is provided thereon, the **semiconductor** elements 3 such as Si and the like and the chip capacitor and the like such as Ta(sub 2)O(sub 5) and the like are mounted on an element-mounting wiring **substrate** 2, on which a wiring **film** 5 is provided using the conductive material such as a metal and the like, and an internal wiring 4 is provided using an Au wire and the like. The **copper** alloy such as tin-**copper** (**Cu**-10% Sn) and the iron material such as 42-alloy (Fe-42% Ni) and the like may be used as the material for the lead part 1 to be used for external connection with which an **Al** and the precious metal **film** 8' is formed at the tip of an inner lead. The **semiconductor** element mounting **substrate** 2 and the external connection lead part 1 are connected with the bonding wire 7 formed with **Al** and the precious metals, and they are sealed with the **synthetic resin** 9 such as **epoxy resin** and the like.

39/3,AB/28 (Item 28 from file: 347)
DIALOG(R)File 347:JAPIO

02031455
TERMINAL CONNECTING STRUCTURE FOR **SEMICONDUCTOR**

PUB. NO.: 61-245555 [JP 61245555 A]
PUBLISHED: October 31, 1986 (19861031)
INVENTOR(s): ANDO MASARU
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 60-086293 [JP 8586293]
FILED: April 24, 1985 (19850424)
JOURNAL: Section: E, Section No. 492, Vol. 11, No. 95, Pg. 11, March 25, 1987 (19870325)

ABSTRACT

PURPOSE: To obtain a terminal connecting structure having high reliability by floating a soldering section for a **Cu** terminal from an AlN **substrate** and soldering the soldering section.

CONSTITUTION: **Al** (sub 2)O(sub 3) powder is suspended into nitrocellulose, thus preparing a liquid having predetermined viscosity. Soldering execution positions 1 for the AlN **substrate** 6 are masked, and a suspension is printed only where corresponding to a **Cu** pattern 2, and also printed on the back. Tough pitch **copper** in thickness of approximately 300.mu.m is placed and heated at a temperature where the hypo-eutectic region of **Cu** is kept in an inactive atmosphere, and cooled, thus manufacturing CuO(sub 2) on an **Al**(sub 2)O(sub 3) **layer** 5. The AlN **substrate** 6 holding an air gap 4 is arranged oppositely to a **Cu layer** 3 in which there is no **Al**(sub 2)O(sub 3) 5. An external terminal 8 is soldered 7 to the **Cu layer** in the upper section of the air gap 4, a **semiconductor** element is fixed to the conductive pattern 2 consisting of CuO to form an assembly, and the terminal 6 is projected and sealed with a **resin**. According to the constitution, stress due to the difference of thermal **expansion coefficients** is absorbed, thus preventing the generation of a **substrate** crack or cleavage and the peeling of the **Cu** pattern

45/3,AB/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02722189
FLEXIBLE PRINTED **SUBSTRATE**

PUB. NO.: 01-019789 [JP 1019789 A]
PUBLISHED: January 23, 1989 (19890123)
INVENTOR(s): NAGANO KOSAKU
NOJIRI HITOSHI
APPLICANT(s): KANEGAFUCHI CHEM IND CO LTD [000094] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-174881 [JP 87174881]
FILED: July 15, 1987 (19870715)
JOURNAL: Section: E, Section No. 756, Vol. 13, No. 198, Pg. 44, May 11, 1989 (19890511)

ABSTRACT

PURPOSE: To improve a dimensional stability without deteriorating a flexibility by a method wherein a **substrate** containing at least a conductor and a insulating material is provided, where the linear **expansion coefficient** and the extensibility of the insulating material are specified.

CONSTITUTION: A flexible printed **substrate** is provided, where an insulating **layer** adheres to a conductor through intermediary of an adhesive agent, a patterning and a etching are performed thereon, and a adhesive agent usedin the manufacture of a usual flexible printed **substrate** can be used. An conductor consists of such a metal as is represented by **copper**, iron, or **aluminum**, or a foil of them, or a material other than them. If the insulating material used as a important material is less than 2.0X10(sup -5)/ deg.C in linear **expansion coefficient** and more than 30% in extensibility when a tensile break takes place, it is usable, where a **synthetic resin**, especially polyimide is desirable. In polyimide, an aromatic polyimide copolymer represented by constitutional formulas A and B is desirable.

48/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00326232 JICST ACCESSION NUMBER: 86A0534783 FILE SEGMENT: JICST-E
Aluminum-nitride DBC **substrate**.
MIZUNOYA NOBUYUKI (1); HATORI MASAKAZU (1)
(1) Toshiba Corp., Yokohama Metal Works
Toshiba Rebyu(Toshiba Review), 1986, VOL.41,NO.9, PAGE.811-814, FIG.7, TBL.2, REF.4
JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The writers have developed AlN-"DBC" **substrate** to be applied to **semiconductor devices**. **Aluminum**-nitride, though high in thermal conductivity, is very difficult to produce high-bonding strength between AlN and **Cu**, because AlN is inferior to oxide ceramic in the activity of wetting **Cu** metal. The writers discovered that forming an intermediate **layer** on an AlN surface effects sufficient bonding strength in bonding **copper** to AlN surface by heat treatment at 1,050-1,100.DEG.C in air atmosphere. This **layer** enables the formation of strong bonding between a **copper** plate and an AlN surface, with a pull strength over 5kg/cm. The strong bonding of the **copper** enhances the inherent characteristics of AlN ceramic: such as high-thermal conductivity, high-electrical insulation capacity, high-dielectric strength and low-dielectric constant. It is made possible to mount Si pellets measuring 10mm square or above direct on AlN-"DBC" **substrate**. The application of AlN-"DBC" to high-power **semiconductor** modules will surely effect simplification of structure and improvement of reliability.(author abst.)

48/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010760325
WPI Acc No: 1996-257280/199626
XRPX Acc No: N96-216429
Heat-dissipation fin for **semiconductor** package, hybrid integrated circuit **substrate** - has several metal fins made by bending rectangular metal plates whose bases are connected to several pores formed on metal board using solder or **adhesive**
Patent Assignee: MITSUBISHI MATERIALS CORP (MITV)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8107166	A	19960423	JP 94241722	A	19941006	199626	B

Priority Applications (No Type Date): JP 94241722 A 19941006
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8107166	A		7	H01L-023/36	

Abstract (Basic): JP 8107166 A

The fin (11) includes a metal structures (22) formed by bending thin rectangular metal plates. The bases (22a) of the metal structures are attached to several pores (21a) formed on a metal board (21) using a solder (14) or an **adhesive** agent.

The metal board consisting of an alloy of **Cu**, W , and Ni connects to the back surface of a ceramic **layer** (16). The ceramic **layer** serves as the bottom **substrate** of a **semiconductor device** (13) and consists of an **Al** metal. The metal board has an area which can cover a thermal **expansion coefficient** equivalent to the ceramic **layer** . A **semiconductor** chip (12) mounts the other surface of the ceramic **layer**.

USE/ADVANTAGE - Also for e.g power module **substrate**. Dissipates heat generated by **semiconductor** chip. Prevents ceramic **substrate** and metal board from breaking and metal fin from deforming.

08/27/2002 10/022,297

52/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6146577 INSPEC Abstract Number: B1999-03-2570P-001
Title: Reliability of direct **copper** bonded (DBC) **substrates** [power packaging]
Author(s): Schulz-Harder, J.; Exel, K.; Franz, H.
Author Affiliation: Curimik Electron. gmbh, Eschenbach, Germany
Conference Title: 11th European Microelectronics Conference. Proceedings p.593-6
Publisher: ISHM-Italy, Pavia, Italy
Publication Date: 1997 Country of Publication: Italy xxii+691 pp.
Material Identity Number: XX-1997-01723
Conference Title: Proceedings of 11th European Microelectronics Conference
Conference Date: 14-16 May 1997 Conference Location: Venice, Italy
Language: English
Abstract: Direct bonded **copper** (DBC) **substrates** based on **Al**/sub 2/O/sub 3//**copper** have been proven in power electronic applications over many years. DBC **substrates** have thick solid **copper layers** with high bonding strength to the ceramic **layer**. The high electrical conductivity and thicknesses of the **Cu layers** allow very high current flows. The **coefficient** of thermal **expansion** of the **Cu** surface is controlled by the high **Cu** to ceramic bond strength and by the much larger elastic modulus of the ceramic. The low CTE of the total **substrate** makes it possible to solder large area Si **semiconductors** directly on to the **Cu** surface without Si damage or solder fatigue by temperature cycling. Older technologies have used a leveling Mo **layer** between **substrate** and Si, but this is not necessary for DBC **substrates**. There is a further advantage of heat spreading in the thick **Cu layer** , which helps to reduce thermal resistance. The DBC bonding process is performed in a temperature range of 1065-1080 degrees C. Solder processes up to 400 degrees C do not significantly impair DBC **substrate** bonding strength. DBC **substrate** thermal conductivity is essentially defined by the ceramic thermal conductivity and thickness. Also, power module thermal resistance is influenced by the **solder layers** between Si chip and **substrate**, and between **substrate** and baseplate. The connection **layer** between baseplate and cooling assembly is also important. It is thus necessary to optimize every stage in power circuit development, with the goal of keeping the Si assembly temperature as low as possible to reach high mean time between failure figures for a high reliability module/package assembly.
Subfile: B

52/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013557456
WPI Acc No: 2001-041663/200106
XRAM Acc No: C01-012154
XRPX Acc No: N01-031152

Substrate for a power **semiconductor** module in an electric vehicle has a buffer **layer** of intermediate thermal **expansion coefficient** interposed between an insulating **substrate** and a heat sink

Patent Assignee: MITSUBISHI MATERIALS CORP (MITV)
Inventor: KUBO K; NAGASE T; NAGATOMO Y; SHIMAMURA S

Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10013189	A1	20001005	DE 1013189	A	20000317	200106	B
JP 2001148451	A	20010529	JP 20002700	A	20000111	200136	
US 6310775	B1	20011030	US 2000531489	A	20000320	200172	

Priority Applications (No Type Date): JP 20002700 A 20000111; JP 9979554 A 19990324; JP 99254259 A 19990908
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10013189	A1		9	H01L-023/14	
JP 2001148451	A		7	H01L-023/373	
US 6310775	B1			H05K-007/20	

Abstract (Basic): DE 10013189 A1
Abstract (Basic):

NOVELTY - A power module **substrate** comprises a buffer **layer** of intermediate thermal **expansion coefficient** interposed between an insulating **substrate** and a heat sink.

DETAILED DESCRIPTION - A power module **substrate** has a buffer **layer** which is interposed between an insulating **substrate** and a heat sink and which has a surface area one to three times larger than that of the **substrate**. The buffer **layer** is formed of a material with a thermal **expansion coefficient** intermediate between those of the **substrate** and the heat sink.

USE - As a **substrate** for a power **semiconductor** module used for controlling high voltages and heavy currents in electric vehicles such as automobiles and trains.

ADVANTAGE - The buffer **layer** reduces thermal stresses on the insulating **substrate**, improves the heat sink cooling efficiency, prevents degradation of the **solder layer** used to mount **semiconductor** chips on the circuit **layer**, reduces production costs (by allowing use of **Al** or **Cu** for the heat sink instead of expensive AlSiC) and increases productivity.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a power module **substrate** according to the invention.

Power module (11)
Insulating **substrate** (12)

52/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012999454
WPI Acc No: 2000-171306/200015
XRAM Acc No: C00-053363
XRPX Acc No: N00-127280
Transferring solder to a **semiconductor device** and/or testing the device involves using a transfer **substrate**
Patent Assignee: MOTOROLA INC (MOTI); FRAUNHOFER GES FOERDERUNG ANGEWANDTEN (FRAU)
Inventor: BUDWEISER W; JUNG E; KASKOUN K
Number of Countries: 087 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200004578	A1	20000127	WO 99EP5033	A	19990714	200015	B
AU 9952833	A	20000207	AU 9952833	A	19990714	200029	
EP 1099247	A1	20010516	EP 99938262	A	19990714	200128	
			WO 99EP5033	A	19990714		
US 6409073	B1	20020625	US 98116140	A	19980715	200246	
			WO 99EP5033	A	19990714		
			US 2001743739	A	20010227		

Priority Applications (No Type Date): US 98116140 A 19980715; US 2001743739 A 20010227
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200004578	A1	E	27	H01L-021/60	
Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZA ZW					
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ UG ZW					
AU 9952833	A			H01L-021/60	Based on patent WO 200004578
EP 1099247	A1	E		H01L-021/60	Based on patent WO 200004578
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE					
US 6409073	B1			B23K-031/02	Cont of application US 98116140 Based on patent WO 200004578

Abstract (Basic): WO 200004578 A1
Abstract (Basic):

NOVELTY - A solder is transferred to a receiving **substrate** by providing a transfer **substrate** having an insulating **layer**, a conductive **layer**, a **solder** receiving stud and a solder bump. The solder bump in its liquid state gets into contact with the solder accepting stud. The transfer **substrate** is then separated from the receiving **substrate** leaving the solder bump on the solder stud.

DETAILED DESCRIPTION - A method for transferring a solder to a receiving **substrate** comprises:

(a) providing a transfer **substrate** (10) having an insulating **layer**, a conductive **layer** (16) that is non-wettable by the solder, a solder receiving stud (22) that is formed of a conductive material, which is wettable by the solder and has a first area, and a solder bump (32) formed on the solder receiving stud;

(b) providing a receiving **substrate** with a solder accepting stud formed of a conductive material;

(c) contacting the solder bump that is in its liquid state and the solder accepting stud (120); and

(d) separating the transfer **substrate** from the receiving **substrate** leaving the solder bump on the solder accepting stud.

INDEPENDENT CLAIMS are also included for:

(A) a method for making a transfer **substrate** useful for transferring a solder to a receiving **substrate**; and

(B) a method for testing a **semiconductor device**.

USE - For transferring solder to a device, e.g. **semiconductor device**.

ADVANTAGE - Facilitates testing of the device. The bulk transfer **substrate** material has a **coefficient** of thermal **expansion** (CTE) similar to the actual device being tested and it can maintain appropriate contact during testing even at elevated temperatures. The transfer **substrate** can be reused after testing and solder transfer to keep **semiconductor** manufacturing cost low. Testing can be performed at either the die or wafer level, and the entire wafer can be tested at once. The **substrate** can be used in conjunction with any type of solder deposition process including the low-cost screen-printing technique. The solder compositions can be used for which no plating method is existing because it enables the use of stencil printing for solder deposition.

DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional illustrations on how the solder transfer **substrate** is used to test a **semiconductor device**.

Transfer **substrate** (10)
Conductive **layer** (16)
Solder receiving stud (22)
Solder bump (32)
Semiconductor device (100)
Solder accepting stud (120)
pp; 27 DwgNo 9/10

52/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004261209
WPI Acc No: 1985-088087/198515
XRAM Acc No: C85-038273
XRPX Acc No: N85-065886
Soldered IC component assembly prodn. - using bond **layer** between insulation and **substrate** to reduce differential thermal expansion
Patent Assignee: SIEMENS AG (SIEI)
Inventor: LAUTERBACH R
Number of Countries: 011 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3335184	A	19850404	DE 3335184	A	19830928	198515	B
EP 139205	A	19850502	EP 84110782	A	19840910	198518	
JP 60092628	A	19850524	JP 84198405	A	19840921	198527	

Priority Applications (No Type Date): DE 3335184 A 19830928
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 3335184	A		13		
EP 139205	A	G			

Designated States (Regional): AT BE CH DE FR GB IT LI NL SE

Abstract (Basic): DE 3335184 A

Semiconductor components, with one or more integrated circuits, are produced by plasma spraying a thin ceramic insulation **layer** on the surface of a metal **substrate**, applying a **solderable layer** onto the insulation **layer**, and then **soldering** the integrated circuit(s) onto the **solderable layer**.

The novelty is that, prior to applying the insulation **layer** (4) to the sand blasted roughened surface (22) of the metal **substrate** (2), a bond **layer** (3) is applied by plasma spraying, the bond **layer** being of a material with a thermal **expansion coefficient** between those of the metal **substrate** and the ceramic insulation. Suitable bond **layer** materials are **Al**-Si alloy, **Cu**, **CU-Al** alloy, **Cu**-Sn alloy, a **Cu**-glass mixt., Ni, Ni-**Al** alloy, Ni-**Al**-Mo alloy, Ni-Cr alloy, Mo and W.

ADVANTAGE - Permanent and reliable adhesion between the insulation **layer** and the metal **substrate** is ensured.

/6

52/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002219934
WPI Acc No: 1979-19109B/197910
Semiconductor device with electrode of **copper** and carbon fibre - **coated** with **solder** resist **film**
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 54013262	A	19790131				197910	B

Priority Applications (No Type Date): JP 7777846 A 19770701

Abstract (Basic): JP 54013262 A

A **semiconductor device** comprises a **semiconductor substrate** and an electrode consisting of mixt. of **copper** and carbon fibre. The electrode is soldered to the **semiconductor substrate**, and the surface of the electrode member except for the surface to be soldered to the **semiconductor substrate** and a header is covered with a **solder** resist **film**. The **solder** resist **film** may comprise silicon nitride, silicon oxide, nickel oxide, alumina, tantalum oxide, Cr, **Al**, W, Mo, titanium oxide, titanium carbide or tungsten carbide.

Since the electrodde member has the same thermal **expansion coefficient** as the **semiconductor substrate**, cracking of the **semiconductor substrate** during soldering and operating can be prevented. The **solder** resist **film** enables **soldering** to be carried out easily.

52/3,AB/6 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03081455
CONNECTING STRUCTURE BETWEEN COMPONENTS OF **SEMICONDUCTOR DEVICE**

PUB. NO.: 02-056955 [JP 2056955 A]
PUBLISHED: February 26, 1990 (19900226)
INVENTOR(s): SASAME AKIRA
SAKAGAMI HITOSHI
TAKEUCHI HISAO
MIYAKE MASAYA
YUSHIO YASUHISA
AKAZAWA HITOSHI
YAMAKAWA AKIRA
APPLICANT(s): SUMITOMO ELECTRIC IND LTD [000213] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-164964 [JP 88164964]
FILED: July 04, 1988 (19880704)
JOURNAL: Section: E, Section No. 927, Vol. 14, No. 225, Pg. 26, May 14, 1990 (19900514)

ABSTRACT

PURPOSE: To prevent the generation of warps and cracks by using soft metals or soft alloys with high plastic deformability, for the join of the connecting structure of base material or covering part material made of **aluminum** nitride with connecting part material for the base material or covering material.

CONSTITUTION: A metallized **layer** 2 is formed on a part of the surface of an **aluminum** nitride **substrate** 1. To this metallized **layer** 2, a lead frame 3 is soldered with metallic solder, etc., and joined. Buffering material 13, made of soft metals such as **copper**, etc., with nickel **solder layers** formed on the surfaces is interposed between the metallized **layer** 2 and lead frame 3. Besides, a **semiconductor** element 4 such as an FFT, etc., with a large amount of heat generation is mounted at a specified position of the **aluminum** nitride **substrate** 1, and it is connected to the metallized **layer** 2 or lead frame 3 with pieces of bonding wire 5. This makes it possible to prevent the generation of cracks or warps, as almost all the stress generated by the difference between the thermal **expansion coefficients** of the **aluminum** nitride **substrate** 1 and connecting part material 3 is absorbed by the plastic deformation of the buffering material 13.

52/3,AB/7 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01611435
SEMICONDUCTOR DEVICE

PUB. NO.: 60-089935 [JP 60089935 A]
PUBLISHED: May 20, 1985 (19850520)
INVENTOR(s): KURIHARA YASUTOSHI
MINAGAWA TADASHI
YATSUNO KOMEI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-197282 [JP 83197282]
FILED: October 21, 1983 (19831021)
JOURNAL: Section: E, Section No. 344, Vol. 09, No. 234, Pg. 161, September 20, 1985 (19850920)

ABSTRACT

PURPOSE: To prevent thermal fatigue at adhered position due to thermal distortion without damaging heat radiation during operation by adhering a **semiconductor substrate** on a metal member using an alloy solder which has main elements of **Al** and Ge.

CONSTITUTION: On a metal support plate 1, e.g., a **copper** plate 1 **coated** with Ni, an Si transistor TR2 is adhered with an alloy **solder layer** 3 consisting of **Al** and Ge. The **coefficient** of thermal **expansion** of the alloy solder has a nearly intermediate value between those of **copper** as the support plate 1 and Si as the main material of TR2 and has an effect of alleviating the difference of the coefficients of these two materials. The alloy solder has also greater mechanical strength and can easily realize a construction in which concentration of thermal stress on the **layer** 3 itself is avoided. The alloy solder has also smaller thermal resistance and is excellent in heat radiation.

55/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7153564 INSPEC Abstract Number: B2002-02-2560R-096
Title: AlSiC baseplates for power IGBT modules: design, performance and reliability
Author(s): Occhionero, M.A.; Fennessy, K.P.; Adams, R.W.; Sundberg, G.J.
Author Affiliation: Ceramics Process Syst., Chartley, MA, USA
Conference Title: PCIM 2001 Power Electronics Conference. Presented at Powersystems World 2001 Conference and Exhibition p.172-7
Publisher: Intertech Publishing, Stamford, CT, USA
Publication Date: 2001 Country of Publication: USA viii+553 pp.
ISBN: 0 87288 799 5 Material Identity Number: XX-2001-00324
Conference Title: Proceedings of PCIM/HFPC 2001. Part of Power Systems World 2001 Show
Conference Date: 11-13 Sept. 2001 Conference Location: Rosemont, IL, USA
Language: English
Abstract: Improved baseplate materials are required to provide superior reliability and heat transfer as IGBT power density increases. The key is for the baseplate thermal **coefficient** of **expansion** (TCE) to be matched to the module design and to have sufficient thermal conductivity (kappa). **Aluminum** silicon carbide (AlSiC), a metal matrix composite material, provides a TCE that is compatible with the attachment of dielectric **substrates** and IGBT silicon devices. Matching the AlSiC baseplate TCE to other materials within the IGBT module can provide more than two times longer module life by minimizing thermal stresses that cause high cycle fatigue failure. A matched TCE also eliminates the need for stress compensating compliant **layers** and expansion graded thick **solders** that increase thermal resistance and complexity of assembly. The TCE of AlSiC can be adjusted for the IGBT module design by control of the SiC volume fraction in the AlSiC composite. The AlSiC average TCE can be controlled between 7.5 and 12 ppm/ degrees C (30 - 150 degrees C). An AlSiC composition was chosen for the IGBT module with a TCE value of 8.39 ppm/ degrees C (30 - 150 degrees C) and a kappa value of 180 W/mK. IGBT modules with AlSiC baseplates, have equivalent power dissipation and more than two-fold increased reliability over the same module with a **Cu** baseplate. The IGBT module reliability improves with the AlSiC baseplate because the TCE is matched to the IGBT module design. **Cu** baseplates have a kappa value of 398 W/mK. However, the **Cu** baseplate TCE of 17 ppm/ degrees C requires thermal stress compensation **layers** between the **Cu** baseplate and the dielectric ceramic. The benefit of the high **Cu** kappa value is not fully realized because of the thermal resistance penalty associated with the stress compensating **layers**. The Ceramics Process Systems AlSiC module baseplates are cost-effectively fabricated to net-shape, attaining close dimensional tolerances with minimal machining. Additionally, this process allows for the fabrication of engineered bow profiles in the cast module base. The AlSiC process flow is also outlined to illustrate how the process is used to fabricate IGBT baseplates with integrated advanced high thermal conductivity (>1000 W/mK) heat-spreading materials and recirculation cooling paths for higher power applications. Design rules, process capability, fabrication and assembly of

08/27/2002 10/022,297

55/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6307295 INSPEC Abstract Number: B1999-09-0170J-038
Title: Measurement on thermal properties of solid **films** in electronic packages
Author(s): Shi, X.Q.; Pang, H.L.J.; Zhou, W.; Yang, Q.J.
Author Affiliation: Gintic Inst. of Manuf. Technol., Singapore
Conference Title: Proceedings of 2nd Electronics Packaging Technology Conference (Cat. No.98EX235) p.308-12
Editor(s): Tay, A.A.O.; Thiam Beng, L.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1998 Country of Publication: USA 361 pp.
ISBN: 0 7803 5141 X Material Identity Number: XX-1999-00947
U.S. Copyright Clearance Center Code: 0 7803 5141 X/98/$10.00
Conference Title: Proceedings of 2nd Electronics Packaging Technology Conference
Conference Sponsor: IEEE CPMT Soc.; ASME; IMAPS; Gintic Inst. Manuf. Technol.; Inst. Mater. Res. & Eng.; Inst. Microelectron.; Nanyang Technol. Univ.; Nat. Univ. Singapore
Conference Date: 8-10 Dec. 1998 Conference Location: Singapore
Language: English
Abstract: A real-time holographic interferometry computer-aided-measurement system for measurement of the thermal properties of solid **films** has been established. The two principal problems of heat loss and edge reflection and their effects on measurement accuracy were analysed. With this new method, **films** commonly used in electronic packages, such as **aluminium**, **copper**, silicon, nickel, molybdenum, 63Sn/37Pb **solder** alloy, and FR-4, with various **coefficients** of thermal **expansion** ranging from 2.5 ppm/ degrees C to 25 ppm/ degrees C and thermal conductivities ranging from 0.2 W/m-K to 380 W/m-K, were measured. The experimental results show that this system has a high measurement accuracy and a wide measurement range for both **coefficient** of thermal **expansion** and thermal conductivity.
Subfile: B

55/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

4940108 INSPEC Abstract Number: B9506-2550F-033
Title: Metallizing and die attaching to CVD diamond
Author(s): Iacovangelo, C.D.; DiConza, P.J.; Jerabek, E.C.; Zarnoch, K.P.
Author Affiliation: Gen. Electr. Corp. Res. & Dev. Center, Schenectady, NY, USA
p.401-12
Editor(s): Murarka, S.P.; Katz, A.; Tu, K.N.; Maex, K.
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA
Publication Date: 1994 Country of Publication: USA xiv+768 pp.
Conference Title: Advanced Metallization for Devices and Circuits - Science, Technology and Manufacturability
Conference Date: 4-8 April 1994 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The high thermal conductivity of diamond (four times that of **copper**) and its low dielectric constant (less than alumina or **aluminum** nitride) makes it a desirable material for electronic **substrates**. The advent of CVD methods for depositing diamond in large areas at reasonable cost has spurred numerous applications for metallized CVD diamond (CVDD). This paper describes several processes developed to provide reliable and stable metallization on CVDD including bond **coats**, diffusion barriers, vias, and **solder** die attach. Transition metals were found to provide well-adhered bond **coats** through carbide formation at the metal/CVDD interface. XPS depth profiles and conductivity measurements of three metallization systems: Ti-Pt-Au, WTi-Au, and Nb-Au after various heat treatments show WTi-Au to be the most stable system. Via filling was accomplished by LPCVD-W and electrolytic **Cu** for high and low aspect ratio holes respectively. The low thermal **expansion coefficient** of CVDD, approximately 1.5 ppm/ degrees C, presents a major challenge for reliable die attach of GaAs (5.85 ppm/ degrees C). A novel concept for a compliant interface on CVDD which can overcome this problem will be presented.
Subfile: B

55/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

4931610 INSPEC Abstract Number: B9506-0170J-003
Title: Direct-bond **copper substrate** shrinks 1500 W frequency converter
Author(s): Maier, P.H.; Jacobsen, J.B.; Moore, M.F.
Author Affiliation: Curamik Electronics, Germany
Journal: Powerconversion & Intelligent Motion vol.21, no.3 p.45-9
Publication Date: March 1995 Country of Publication: USA
CODEN: PIMOEN ISSN: 0885-0259
Language: English
Abstract: Direct-bond **copper substrates** allow the direct mounting of **semiconductor** dice with good thermal conductivity paths that enable a compact frequency converter power module to meet its power cycling requirements. (DBC) **substrate** that enables a reduction in power module size. At Grundfos the target was to develop a power hybrid module for a frequency converter with a price/performance/space ratio 5 to 10 times better than the market standard. The hybrid module is a compact frequency converter for handling 1500 W at case temperature up to 900 C. A number of technologies were necessary to solve the isolation and thermal problems within the narrow space. A Curamik direct-bond **copper** (DBC) **substrate** technique was used to dissipate the heat from the power dice in the power module. Usually DBC **substrates** are two-dimensional items that look very much like thick **film substrates**. With the Curamik approach the main difference is the thick (0.008 to 0.020-in.) **copper layer** on both sides bonded by a eutectic melt of a thin **copper** oxide **layer**. This is achieved at about 1070 degrees C in a nitrogen atmosphere. This **copper**/ceramic bond provides a very good adhesion to the **Al** /sub 2/O/sub 3/ ceramic. One advantage of this technique is a thermal **coefficient** of **expansion** that is close to that of **Al** /sub 2/O/sub 3/. The ceramic controls the horizontal expansion of the **copper**, so it is possible to **solder** even large area dice directly onto the circuit without exposing the chip to high mechanical stresses.
Subfile: B

55/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

4592032 INSPEC Abstract Number: B9403-2550F-023
Title: Metallizing CVD diamond for electronic applications
Author(s): Iacovangelo, C.D.; Jerabek, E.C.
Author Affiliation: Phys. Chem. Lab., GE Corp. Res. & Dev. Center, Schenectady, NY, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.2105 p.132-8
Publication Date: 1993 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: 1993 International Symposium in Microelectronics
Conference Sponsor: SPIE; ISHM
Conference Date: 9-11 Nov. 1993 Conference Location: Dallas, TX, USA
Language: English
Abstract: Diamond with a thermal conductivity four times that of **copper** and a dielectric constant less than alumina or **aluminum** nitride has long been recognized as a desirable material for electronic **substrates** . The advent of methods for chemical vapor deposition of diamond (CVDD) over large areas at reasonable cost has spurred numerous applications for metallized CVDD. This paper describes several methods developed to provide reliable metallization processes for CVDD, including transition metal bond **coats**, diffusion barriers, patterning, and **solder** die attach. Transition metals e.g. Ti, W, Cr, Nb have been found to provide well-adhered, reliable, and stable bond **coats** through carbide formation at the CVDD interface. The low thermal **expansion coefficient** of CVDD (approximately 1.5 ppm/ degrees C) presents a major challenge for reliable die attach of GaAs; (5.85 ppm/ degrees C). Successful die attach has been achieved with AuSn **solder** and small GaAs dies (2*2 mm). Successful die attach of larger dies (12*12 mm) has been achieved with a novel compliant interface.
Subfile: B

55/3,AB/6 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04823397 JICST ACCESSION NUMBER: 01A0357948 FILE SEGMENT: JICST-E
Establishment of Mass Production Process of AlN **Substrate** with **Copper** Circuit by Active Metal Brazing Method for High Power Module.
NAKAMURA M (1); FUSHII Y (1); TSUJIMURA Y (1); UCHINO K (1)
(1) Denki Kagaku Kogyo
FC, 1999, VOL.1999, PAGE.15-16, FIG.4, REF.8
JOURNAL NUMBER: L0938AAT
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2 666.5/.6
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Regarding the mass production technique of AlN **substrates** with **copper** circuits, following is the points of "whole bonding-full etching method". (1) We have solved some problems such as protrusion of brazing materials, displacement, defect in the bonding process and the yield has been much improved compared with "preformed **copper** pattern method". (2) We were able to use roll **coaters** instead of screen printing in the process of brazing material printing and have improved in **coating** brazing materials to AlN. (3) As we were able to etch **copper** plates and brazing materials separately in the process of removing unnecessary **copper** plates and brazing materials, we could leave a little bit of brazing material at the edge of **copper** pattern as shown in Figure 4. Consequently thermal stress caused by the difference in heat **expansion coefficient** between **copper** plate and AlN **substrate** was reduced and reliability on AlN **substrates** with **copper** circuits has been improved. As you have seen so far, we have established a manufacturing process, superior in mass production, which has never been attained by conventional technique and gained high appreciation from customers. We also have improved reliability of **semiconductor devices** and expanded the area for which we could apply AlN **substrates** with **copper** circuits. Furthermore, by applying this technique, we have succeeded in developing AlN **substrates** with **copper** circuits which have much higher reliability than conventional products and high strength Si3N4 **substrates** with **copper** circuits. (author abst.)

55/3,AB/7 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014418289
WPI Acc No: 2002-238992/200229
Related WPI Acc No: 1999-429575; 2002-074208
XRAM Acc No: C02-071978
XRPX Acc No: N02-184257
Fabrication of contact structure(s) for engaging bumped **semiconductor devices**, by forming masking blocks on **substrate**, undercutting masking block to form contact structure(s), and forming second mask on contact structure
Patent Assignee: AKRAM S (AKRA-I); WARK J M (WARK-I)
Inventor: AKRAM S; WARK J M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010054771	A1	20011227	US 97828255	A	19970326	200229 B
			US 99305493	A	19990505	
			US 2001935494	A	20010823	

Priority Applications (No Type Date): US 97828255 A 19970326; US 99305493 A 19990505; US 2001935494 A 20010823
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010054771	A1		19	H01L-023/48	Cont of application US 97828255 Cont of application US 99305493 Cont of patent US 5929521 Cont of patent US 6291897

Abstract (Basic): US 20010054771 A1
Abstract (Basic):
NOVELTY - A contact structure(s) is fabricated by forming contact areas including masking blocks on a carrier **substrate** (506), undercutting masking block to form contact structure(s), forming a second mask on the contact structure, and undercutting the **substrate** to further define the contact structure(s). The second mask is shorter and narrower than the contact structure.
USE - For the fabrication of contact structure including contact pads (508) for engaging **solder** balls of bumped **semiconductor devices**, e.g., bumped die and bumped packaged integrated circuit device.
ADVANTAGE - The method reduces or eliminates damaging deformation of the **solder** ball, and does not form closed cavities in the **solder** ball surface. It enhances contact-to-**solder** ball connection and accommodates height variations between balls.
DESCRIPTION OF DRAWING(S) - The figure shows an enlarged, partial sectional view of the carrier **substrate** bearing the contact structure.
Carrier **substrate** (506)
Contact pads (508)
Projections (510)

55/3,AB/8 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013137924
WPI Acc No: 2000-309796/200027
XRPX Acc No: N00-232314
Bump structure for **semiconductor device**
Patent Assignee: SEIKO EPSON CORP (SHIH)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000091371	A	20000331	JP 98259035	A	1998091	200027	B

Priority Applications (No Type Date): JP 98259035 A 19980911
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000091371	A		4	H01L-021/60	

Abstract (Basic): JP 2000091371 A
Abstract (Basic):
NOVELTY - A **solder** bump (26) is formed on the surroundings of a pillared **copper** bump (24). The pillared **copper** bump is provided to the pad polar zone of a silicon **substrate** (11). An **aluminium** pad (14), provided between a passivation **film** (13) and a silicon oxide **film** (12), enables the input and output of source voltage of a circuit.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a **semiconductor device** manufacture.
USE - For **semiconductor device**.
ADVANTAGE - Absorbs the stress generated according to the difference of the thermal **expansion coefficient**. Increases shear strength since the **solder** cross section of the section without a pillared metal bump.
DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the **semiconductor device**.
Silicon **substrate** (11)
Silicon oxide **film** (12)
Passivation **film** (13)
Aluminium pad (14)
Pillared **copper** bump (24)
Solder bump (26)
pp; 4 DwgNo 2/5

55/3,AB/9 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012095692
WPI Acc No: 1998-512603/199844
XRAM Acc No: C98-154301
XRPX Acc No: N98-400313
Heat dissipation **substrate** for mounting IGBT, SIT - has insulated **substrate** comprising particle mixture of low thermal expansion carbonisation silicon material and high thermal conductive **copper** material
Patent Assignee: TOYOTA JIDOSHA KK (TOYT)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 10223810	A	19980821	JP 9723889	A	19970206	199844	B

Priority Applications (No Type Date): JP 9723889 A 19970206
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10223810	A		6	H01L-023/373	

Abstract (Basic): JP 10223810 A
The heat dissipation **substrate** (10) consists of a heat sink (11) and an insulated **substrate** (12). The insulated **substrate** consists of fine particle mixture of low-thermal expansion carbonization silicon material and high-thermal conductive **copper** material. **Copper layer** of 0.15mm thickness is formed on the upper and lower sides of the insulated **substrate**.
The insulated **substrate** is connected to power **semiconductor device** (21) on the upper side and heat sink on the lower side of **solder** (14). The heat sink is made of metal plates like **aluminium** and **copper**.
ADVANTAGE - Maintains **coefficient** of linear **expansion**. Secures favourable **soldering** state.
Dwg.1/4

55/3,AB/10 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011153852
WPI Acc No: 1997-131776/199712
Related WPI Acc No: 1996-116108
XRAM Acc No: C97-042491
XRPX Acc No: N97-108853

Copper@ composites to ceramic **substrates** bond for e.g. heat sinks - comprises **copper** composite with **copper** diffused region, and **copper-copper** oxide eutectic **layer** on surface bonded to ceramic member

Patent Assignee: HUGHES AIRCRAFT CO (HUGA)
Inventor: CAMPBELL W T; KRUM A L

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5601932	A	19970211	US 94268488	A	19940630	199712	B
			US 95554580	A	19951106		

Priority Applications (No Type Date): US 94268488 A 19940630; US 95554580 A 19951106
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5601932	A		4	B32B-015/20	Div ex application US 94268488 Div ex patent US 5490627

Abstract (Basic): US 5601932 A

A metal-ceramic structure comprises: (a) a **copper** composite **substrate** having a diffused **Cu** region adjacent the surface; (b) a **copper-copper** oxide eutectic **layer** formed on the **substrate**; and (c) a ceramic member bonded to the eutectic **layer**. Pref. the **copper** composite comprises **copper** -tungsten, or **copper**-molybdenum. Pref. the ceramic comprises alumina, beryllia or **aluminium** nitride.

USE - Used as heat sinks in electronic circuits having ceramic **substrates**, and in fabrication of hybrid circuits in **semiconductor** applications.

ADVANTAGE - Strong bonding is achieved between the **copper** composite and the ceramic, brazing or **soldering** are not required, and the metal and the ceramic have similar **coefficients** of thermal **expansion**.

Dwg.3/3

55/3,AB/11 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007288683
WPI Acc No: 1987-285690/198741
XRAM Acc No: C87-121099
XRPX Acc No: N87-214129
Copper coated iron alloy laminate - with high thermal conductivity, allowing high density IC device mounting
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: MANNS W G; SPINELLI T S; WEIRAUCH D F
Number of Countries: 006 Number of Patents: 003
Patent Family:

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EP 240746	A	19871014	EP 87103300	A	19810907	198741	B
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			EP 87103300	A	19810907		
DE 3177304	G	19940127	DE 3177304	A	19810907	199405	
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EP 240746	A	E	28		
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EP 240746	B1	E	11	H01L-023/52	Related to application EP 81304070
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DE 3177304	G			H01L-023/52	Based on patent EP 240746

Abstract (Basic): EP 240746 A
A metal laminate, for use in a **substrate** for mounting an electronic **semiconductor** component, comprises a flat sheet having a low thermal **expansion coefficient** iron alloy core **layer** with a **copper layer** on each primary face, the laminate having a high thermal conductivity so that, in use, it maintains the component at a safe temp..
USE/ADVANTAGE - The laminate is esp. useful in interconnecting ceramic chip-carrier types of IC devices and direct-mounted ICs, to permit high density device mounting on a low cost **substrate** while avoiding interconnection-bond integrity problems and heat dissipation problems.
Dwg.0/27
Abstract (Equivalent): EP 240746 B
A metal **layer** means for use in a **substrate** on which an electronic **semiconductor** component is to be mounted, the metal **layer** means comprising a flat sheet material having a **layer** of an iron alloy of low thermal **expansion coefficient** having on a primary face thereof a **layer** of **copper**, for facilitating **soldering**, the iron alloy being a member of one of one of the groups of alloys having the following nominal composition by weight: nickel 36 to 50%, balance iron nickel 31%, chromium 8%, cobalt 8%, balance iron nickel 32%, chromium 7%, balance iron chromium 17%,

balance iron chromium 16.5%, **aluminium** 4.5%, balance iron cobalt 57%, chromium 9%, balance iron nickel 23 to 30%, cobalt 17 to 30%, manganese 0.6 to 0.8%, balance iron.

Dwg.1/21

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SEMICONDUCTOR DEVICE

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PUBLISHED: August 17, 1989 (19890817)
INVENTOR(s): KASHIWAGI SHUNJI
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JOURNAL: Section: E, Section No. 845, Vol. 13, No. 507, Pg. 153, November 14, 1989 (19891114)

ABSTRACT

PURPOSE: To form a **semiconductor device** for high frequency amplification which is stable for thermal shock and has high reliability, by making an intermediate **layer** by using metal material whose thermal **expansion coefficient** has an intermediate value between the thermal **expansion coefficients** of an input matching circuit **substrate** and an output matching circuit **substrate**, and that of a casing.

CONSTITUTION: For the intermediate **layer** 5 of a **semiconductor device** for high frequency amplification, a metal material is used, whose thermal **expansion coefficient** has an intermediate value between the thermal **expansion coefficients** of an input matching circuit **substrate** 3 and an output matching circuit **substrate** 4, and that of a casing 1. For example, **copper** (**Cu**) is used for the material of the casing 1. Alumina (**Al**(sub 2)O(sub 3)) is used for the input matching circuit **substrate** 3, the output matching circuit **substrate** 4 and an external terminal connection block 6, and 42 alloy (42 Ni-Fe) is used for the intermediate **layer** 5. The joining between the the casing 1 and the intermediate **layer** 5 is done by AuGe **soldering**. The joining between the intermediate **layer** 5 and the input matching circuit 3 is done by AuSn **soldering**. The joining between the casing 1 and the external terminal connection block 6 is done by Ag **soldering** . Thereby, the destruction of the input and output matching circuits 3, 4, and cracks of the external terminal connection block 6 due to thermal shock can be prevented.